

Compal Confidential

FH5LI MB Schematic Document

LA-J801P

Rev:1.0

2019.10.30

| | | | | | |
|---|------------|--------------------|------------|-----------------------------------|------------------------------------|
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| Issued Date | 2017/11/23 | Deciphered Date | 2018/09/01 | Title | Cover Sheet |
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| | | | | Date: Wednesday, October 30, 2019 | Rev 1.0 |
| | | | | Sheet 1 of 102 | |

HDMI Conn.



page 40

DDI2
HDMI x 4 lanes

eDP



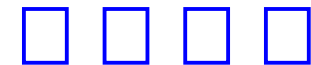
page 38

eDP

DDI

Interleaved Memory

DDR4-ON BOARD 4G 8Gbx16



page 24

260pin DDR4-SO-DIMM X1



page 23

Memory BUS
Dual Channel

1.2V DDR4 2666/3200

USB 3.0
conn x1
USB3 port 1
USB2 port 1

page 72

USB 2.0
conn x2
USB2 port3 (MB)
USB2 port4(SUB)

page 71

CMOS
Camera
USB2 port 7

page 38

Card Reader
RTS5140
Reserved

USB2 port 8(SUB)

Finger
Printer
USB2 port 5

Intel Ice Lake U

Processor

Ice Lake PCH-LP

50x25 mm

15W

1526pin BGA
page 06~19

ICL-U 4+2

eSPI BUS

CLK=24MHz

ENE
KB9052

page 58

Int.KBD



page 63

Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)

page 63

USBx8 48MHz

HD Audio

3.3V 24MHz

SPI

SPI ROM
128Mb page 9HDA Codec
ALC255 page 56Touch
ScreenUSB2 port 6
page 38

Int. Speaker

page 56

Int. DMIC
on Camera
page 38

UAI

page 56

SATA Gen 3
6.0 Gb/s
(SATA2)page 68
PCIe 3.0 x4
8GT/s
Port 13-16

Flexible IO

SATA Gen 3
6.0 Gb/s
port 0
(SATA0)SATA Gen 1
1.5 Gb/s
port 1
(SATA1A)SATA HDD
Conn.

page 67

SATA ODD
Conn.LAN(GbE)
Realtek 8111H
page 51

RJ45 conn.



RTC CKT.

page 11

Power On/Off CKT.

page 63

DC/DC Interface CKT.

page 78

Power Circuit DC/DC

Vinafix.com

page 81~100

Fan Control

page 77

Sub Board

LS-H781P
IO/B

page 73

LS-H783P
LID/B

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| | | | | |
|---|---------------------------|-----------------|--------------------------|----------------|
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| Size | Custom | Document Number | FHSLI M/B LA-H801P | |
| Date: | Tuesday, October 15, 2019 | Sheet | 2 | of 102 |
| Rev | 1.0 | | | |

| | | | | | | |
|----------|-------------|----------------------|----------------------|----------------------|-------------|--------------|
| Vcc | 3.3V +/- 5% | | | | | |
| Ra | 100K +/- 1% | | | | | |
| Board ID | Rb | V _{BID} min | V _{BID} typ | V _{BID} max | EC AD3 | PCB Revision |
| 0 | 0 | 0 V | 0 V | 0.300 V | 0x00 - 0x13 | 0.1 (EVT) |
| 1 | 12K +/- 1% | 0.347 V | 0.345 V | 0.360 V | 0x14 - 0x1E | 1.0 (PVT) |
| 2 | 15K +/- 1% | 0.423 V | 0.430 V | 0.438 V | 0x1F - 0x25 | 1.0 (MP) |
| 3 | 20K +/- 1% | 0.541 V | 0.550 V | 0.559 V | 0x26 - 0x30 | |
| 4 | 27K +/- 1% | 0.691 V | 0.702 V | 0.713 V | 0x31 - 0x3A | |
| 5 | 33K +/- 1% | 0.807 V | 0.819 V | 0.831 V | 0x3B - 0x45 | |
| 6 | 43K +/- 1% | 0.978 V | 0.992 V | 1.006 V | 0x46 - 0x54 | |
| 7 | 56K +/- 1% | 1.169 V | 1.185 V | 1.200 V | 0x55 - 0x64 | |

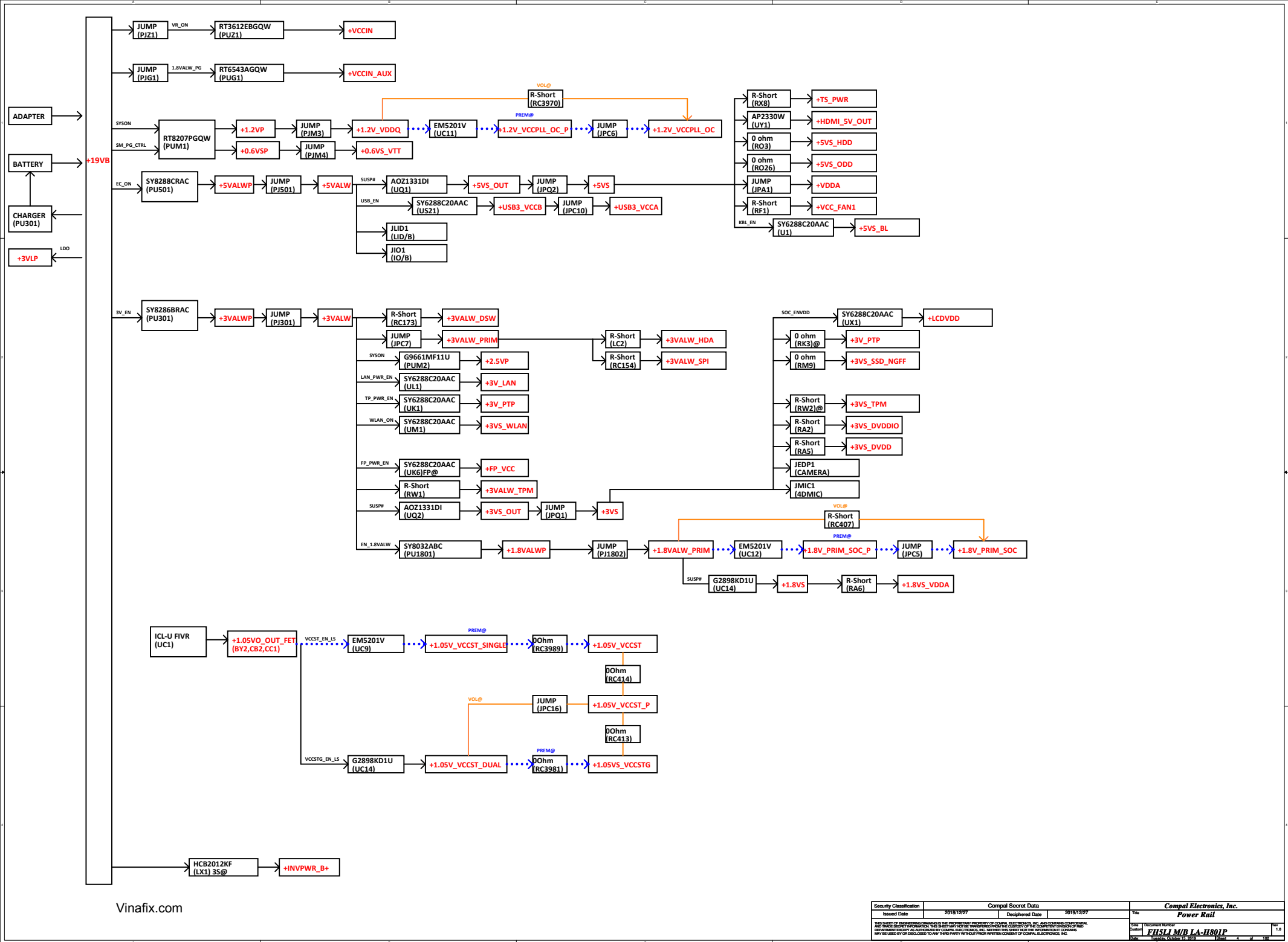
| BOM Option Table | |
|-------------------------|--|
| Item | BOM Structure |
| Unpop | @ |
| Connector | CONN@ |
| G Sensor | GSEN@ |
| CODEC | 255@/256@ |
| For over 3 cell battery | 35@ |
| For Intel CMC | CMC@ |
| CNVi | CNVi@ |
| EMI/ESD requirement | EMC@ / XEMC@ |
| BOM select | 15@ |
| RF requirement | @RF@ |
| TPM | TPM@ |
| Finger Print | FP@/FPEMC@ |
| Finger print power | FP3V@/FP5V@ |
| SATA/ODD select | RD@/NRD@/ODD@ |
| MD BOM Select | NOX76@/X76DSAM@/ X76DMIC@/X76DHYN@/ |
| Memory related | SPD@/DDP@/MEM@ |
| MB Stage | EVT@/DVT@/PVT@/MP@ |
| Premium/Volume | PREM@/VOL@ |
| CPU | i3@/i5@ |
| DAZ | PCB@ |

[illegible]

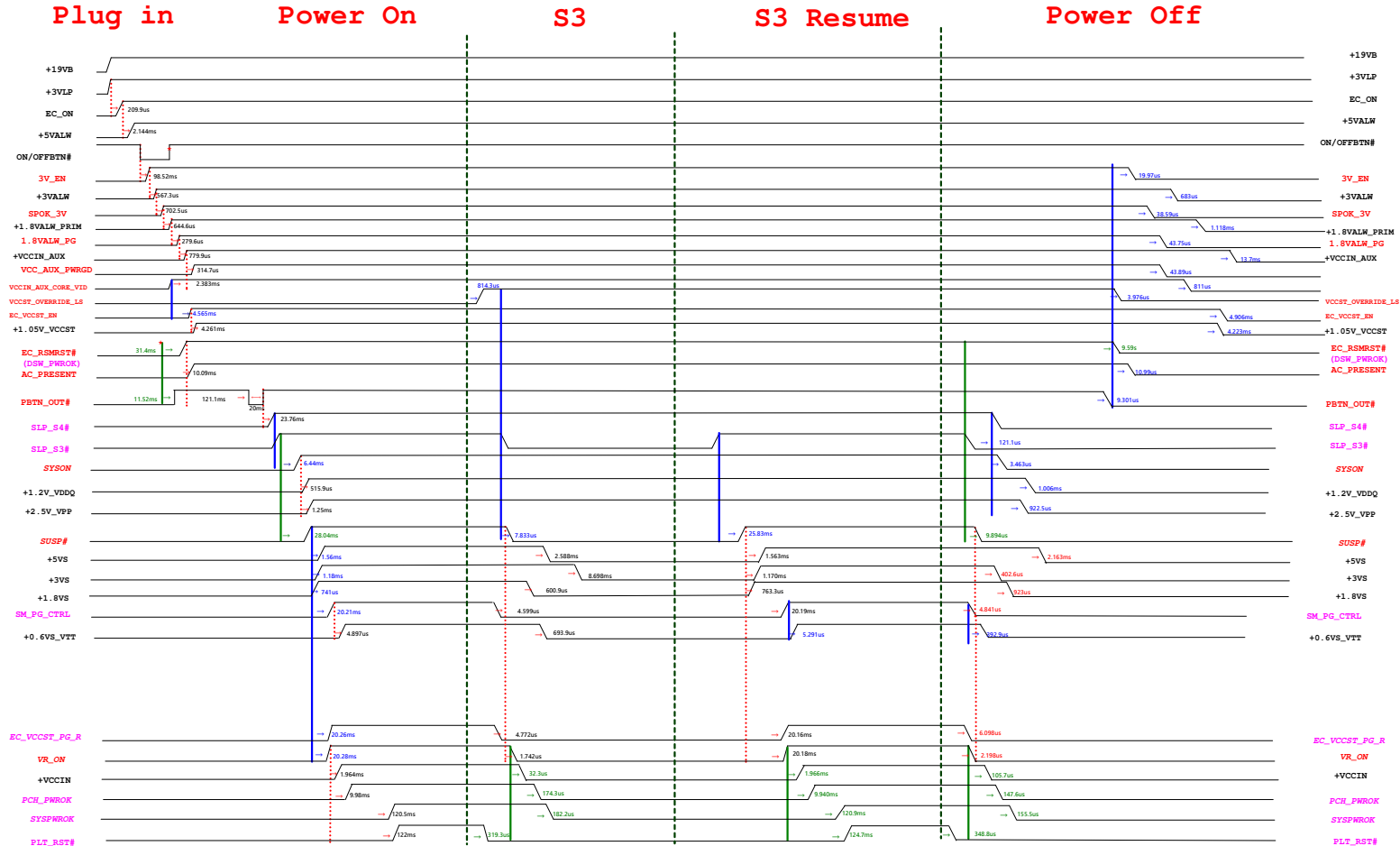
| SIGNAL STATE | SLP_S3# | SLP_S4# | SLP_S5# | +VAL# | +V | +VS | Clock |
|----------------------|---------|---------|---------|-------|-----|-----|-------|
| S0 (Full ON) | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | ON | OFF | OFF | OFF |

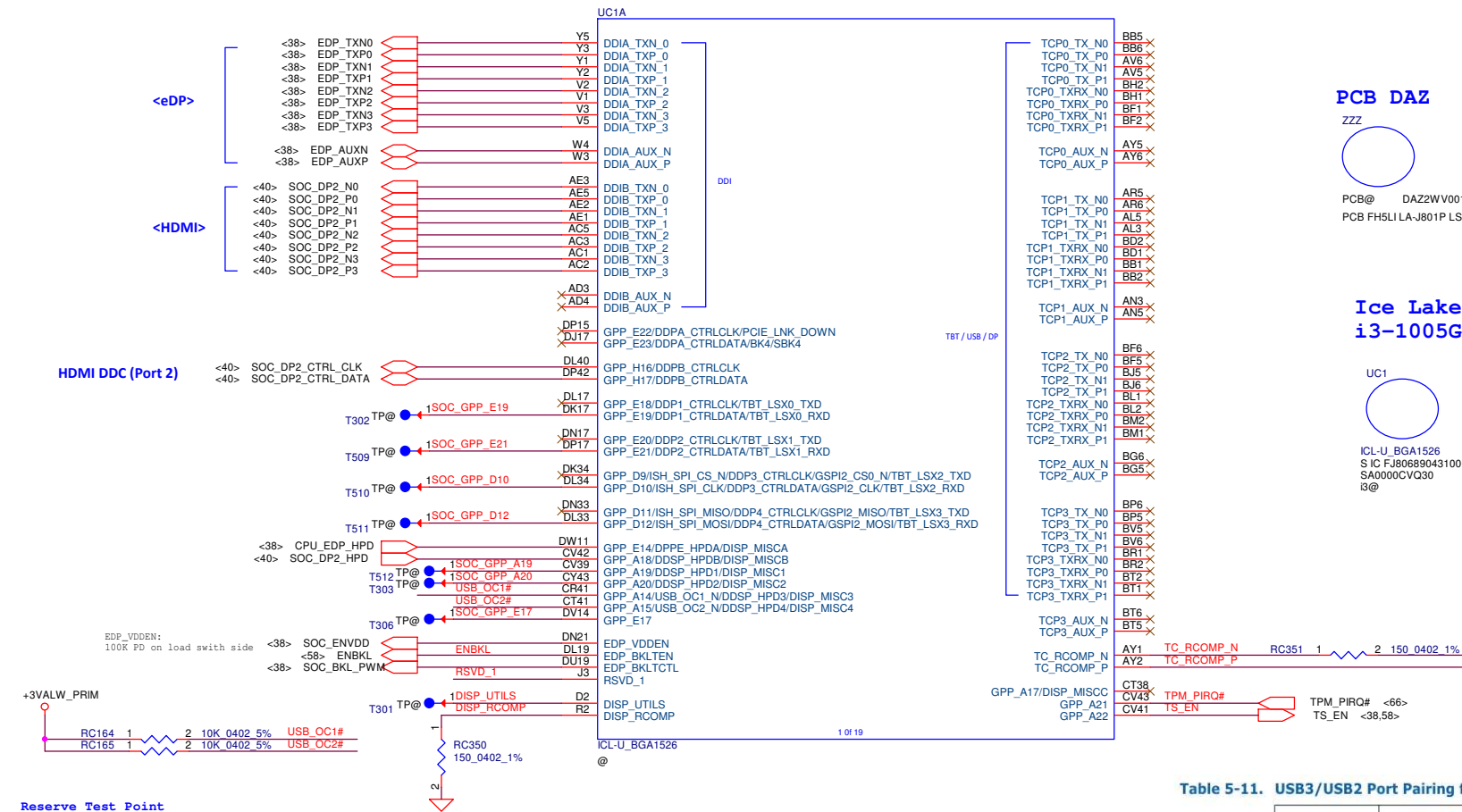
| Power Plane | Description | S0 | S3 | S4/S5 |
|-----------------|--|-----|--------|-------|
| +19V_VIN | Adapter power supply | N/A | N/A | N/A |
| +12.6V_BATT | Battery power supply | N/A | N/A | N/A |
| +19VB | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +VCCIN | Core voltage for CPU | ON | OFF | OFF |
| +VCCIN_AUX | CPU and PCH merged auxiliary power rail | ON | OFF | OFF |
| +0.6VS_VTT | DDR +0.6VS power rail for DDR terminator . | ON | OFF | OFF |
| +1.05VO_OUT_FET | FIVR output of PCH to platform 1.05V Power Gates | ON | ON | OFF |
| +1.05V_VCCST | Sustain voltage for CPU standby modes | ON | ON | OFF |
| +1.05VS_VCCSTG | Gated sustain voltage for CPU standby modes | ON | OFF/ON | OFF |
| +1.2V_VDDQ | DDR4 +1.2V Power Rail | ON | ON | OFF |
| +1.2V_VCCPLL_OC | 1.2V power rail for CPU digital PLL | ON | ON | OFF |
| +1.8VALW_PRIM | +1.8V Always power rail | ON | ON | ON*1 |
| +1.8VS | System +1.8V power rail | ON | OFF | OFF |
| +3VLP | +19VB to +3VLP power rail for suspend power | ON | ON | ON |
| +3VALW | System +3VALW always on power rail | ON | ON | ON*1 |
| +3VALW_PRIM | +3VALW power for PCH suspend rails | ON | ON | ON*1 |
| +3VS | System +3V power rail | ON | OFF | OFF |
| +5VALW | +5V Always power rail | ON | ON | ON |
| +5VS | System +5V power rail | ON | OFF | OFF |
| +RTCVCC | RTC Battery Power | ON | ON | ON |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF
ON*2 power plane is ON when DGPU turn on



FH5LI_EVT Power Sequence AC mode
BIOS ver: V0.01T015
EC: ver: V0.01T08B





PCB DAZ

ZZZ

PCB@ DAZ2WV00100
PCB FH5LI LA-J801P LS-H781P/H783P

Ice Lake-U CPU SKU i3-1005G1

UC1

ICL-U_BGA1526
S IC FJ8068904310007 SRGKF D1 1.2G FCBGA
SA0000CVQ30
i3@

i5-1035G1

UC1

ICL-U_BGA1526
S IC FJ8068904368700 SRGKG D1 1G FCBGA
SA0000CUQ20
i5@

Table 5-11. USB3/USB2 Port Pairing for USB Type-C Connectors

| | Connector C0 | Connector C1 | Connector C2 | Connector C3 |
|----------------|--------------|--------------|--------------|--------------|
| CPU USB3 port# | 1 | 2 | 3 | 4 |
| PCH USB2 port# | 2 | 3 | 4 | 6 |

To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.

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| Rev | | 1.0 | | FHSI M/B LA-H801P | | | | | | | |

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Reserve Test Point

GPP_E19
TBT LSX #0 PINS VCCIO CONFIGURATION
NO INTERNAL PU/PD

HIGH: 3.3V
LOW: 1.8V

GPP_E21
TBT LSX #1 PINS VCCIO CONFIGURATION
INTERNAL PD 20K

HIGH: 3.3V
LOW: 1.8V

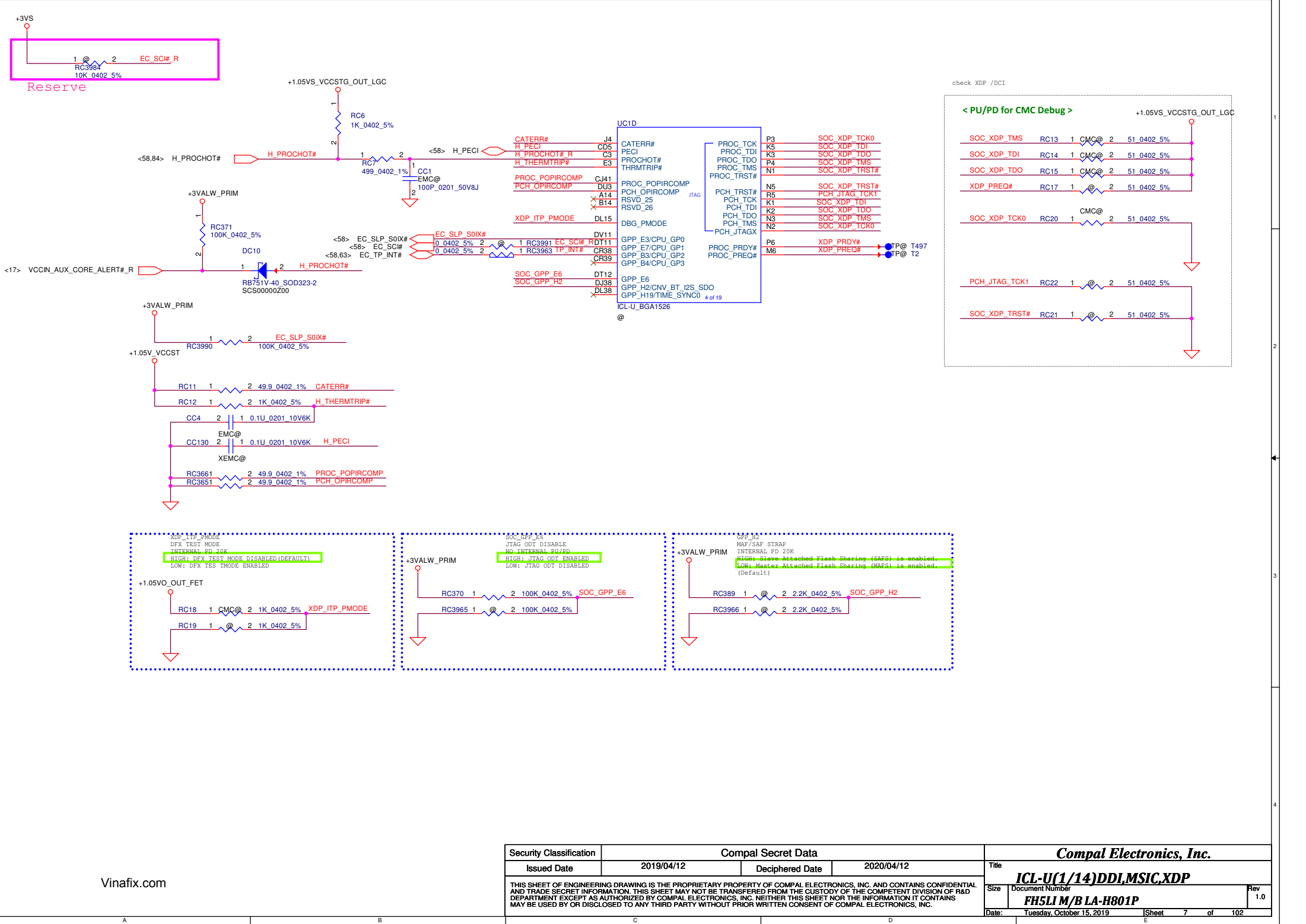
GPP_D10
TBT LSX #2 PINS VCCIO CONFIGURATION
NO INTERNAL PU/PD

HIGH: 3.3V
LOW: 1.8V

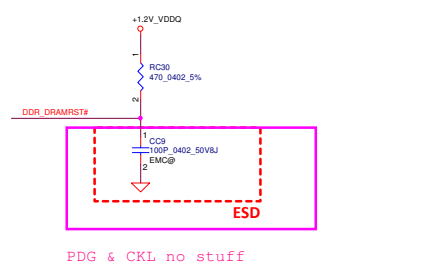
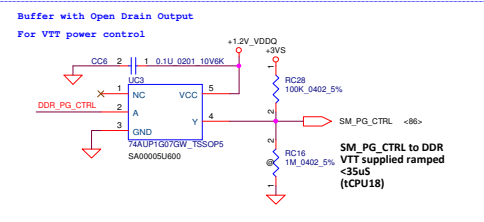
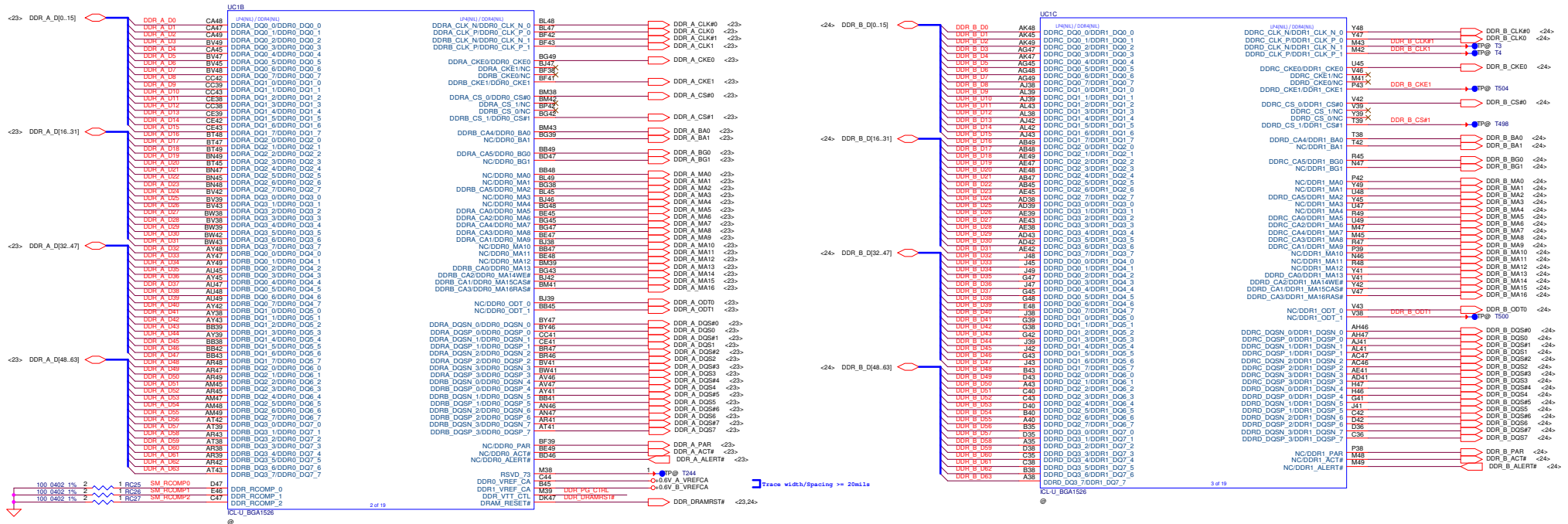
GPP_D12
TBT LSX #3 PINS VCCIO CONFIGURATION
NO INTERNAL PU/PD

HIGH: 3.3V
LOW: 1.8V

Vinafix.com

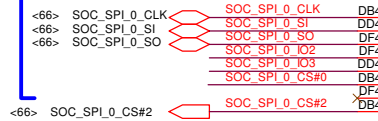


DDR4: Refer to 575034_ICL_U42_DDR4_T3_6L_Core_Schematics_Rev0p7

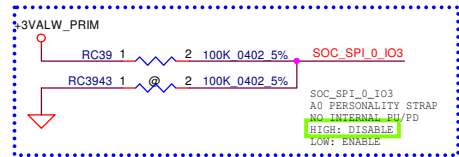
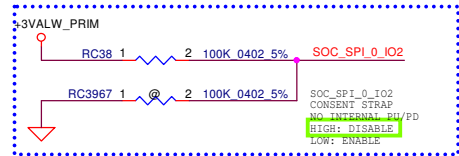
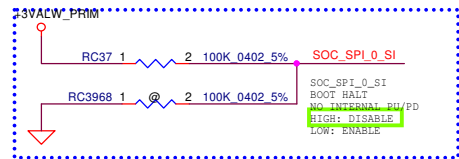
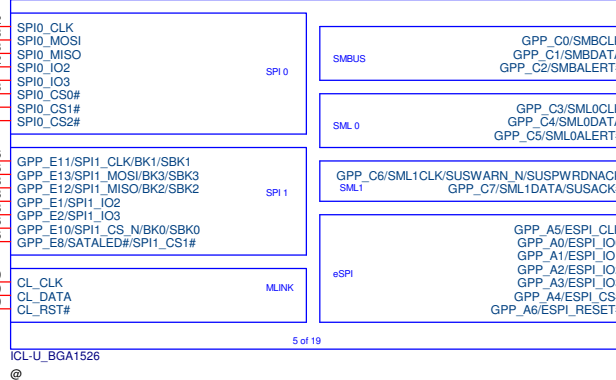


SPI ROM

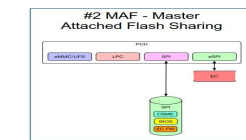
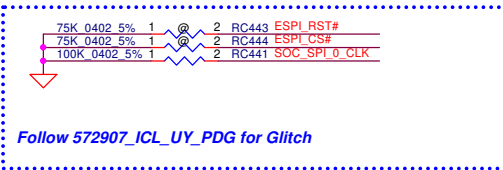
TPM<-



UC1E

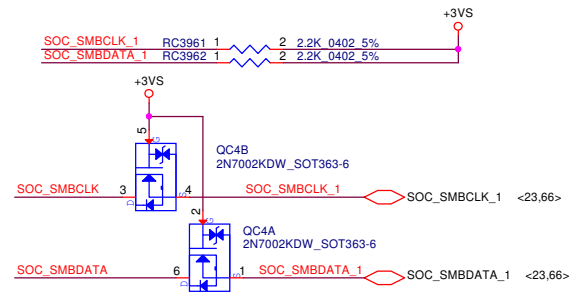
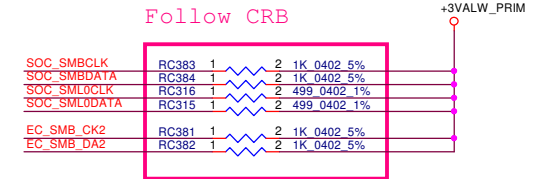


| | | | |
|------------------|----------|------------------------|---|
| SPI0_MOSI | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
| SPI0_IO2 | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |
| SPI0_IO3 | Reserved | Rising edge of RSMRST# | External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling. |

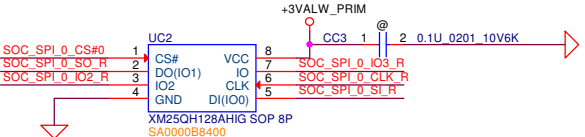


MAF - Master Attached Flash
Single SPI Flash attached to SPI Bus
EC FW access through eSPI Bus

Follow CRB

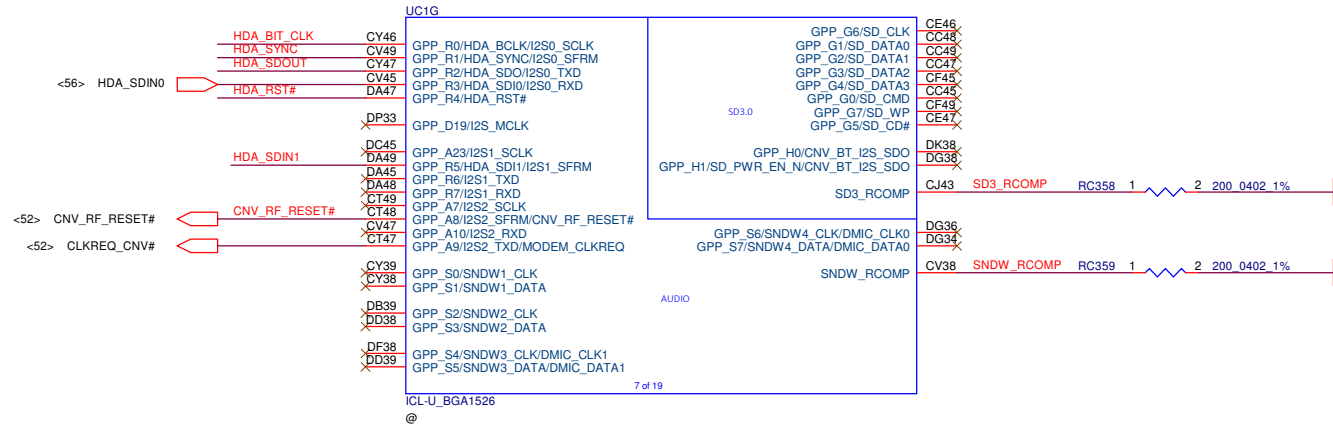


< SPI ROM - 16M >

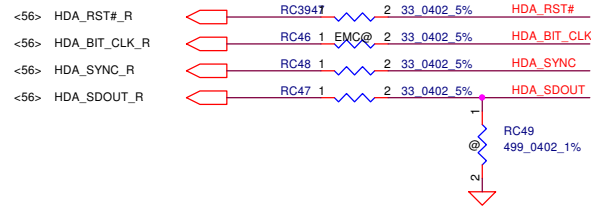


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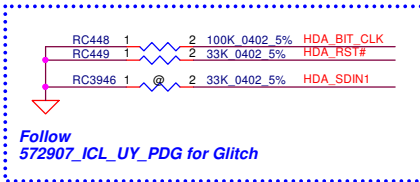
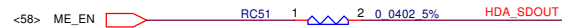
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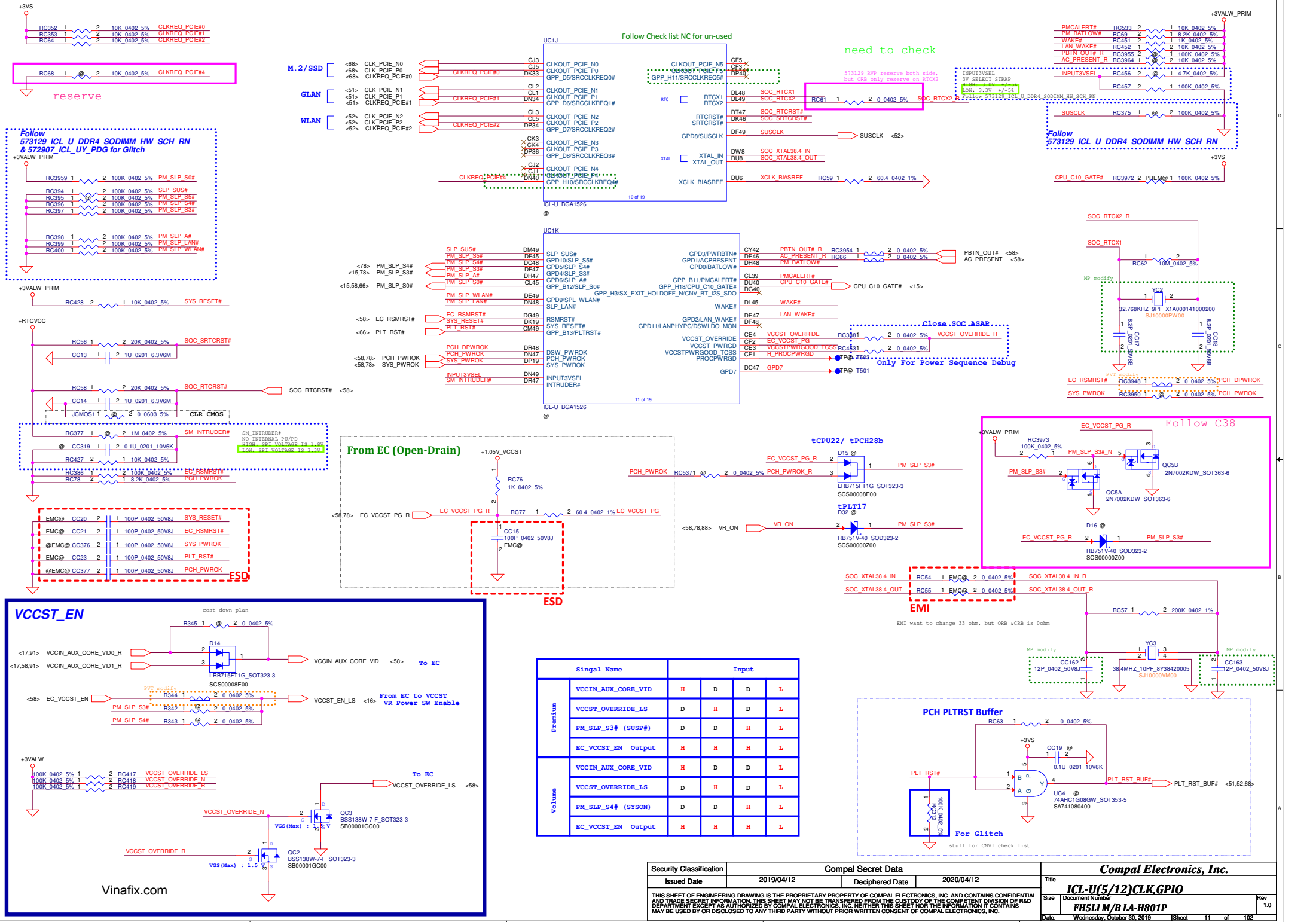
< HD AUDIO >

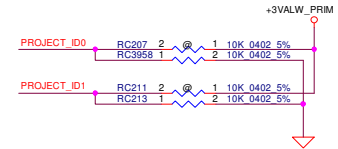
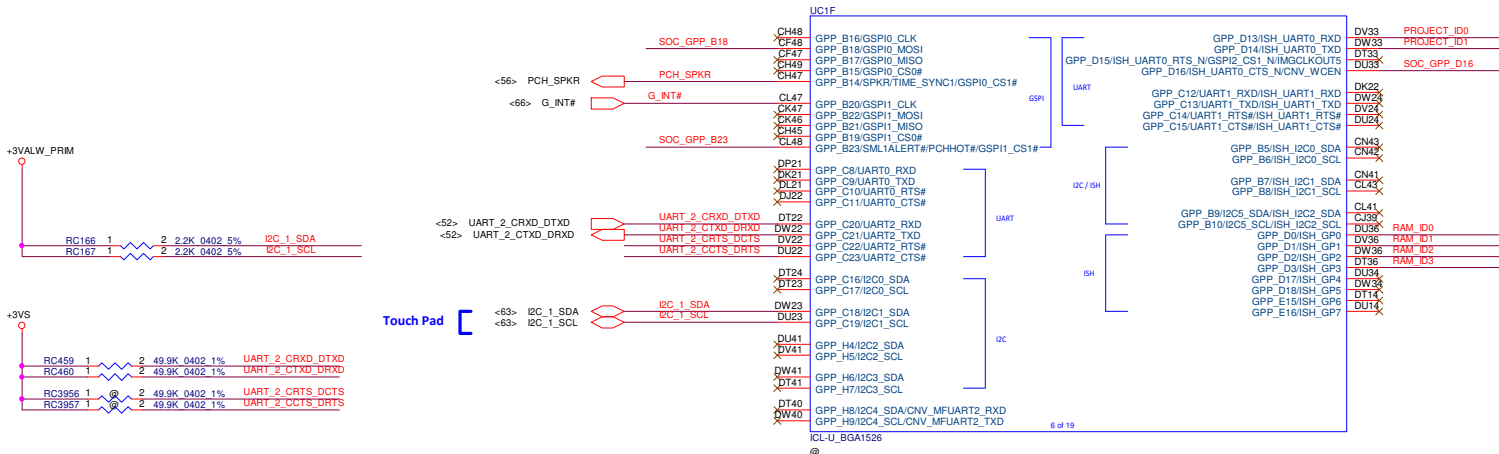


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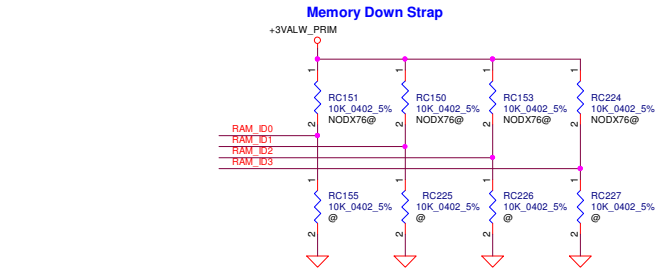


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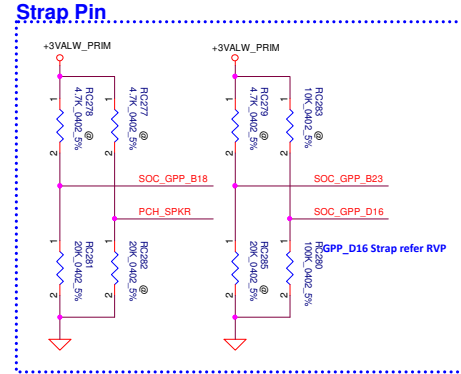




| Project ID | Project_ID1 GPP_D14 | Project_ID0 GPP_D13 |
|------------|------------------------|------------------------|
| * FHSLI | 0 | 0 |
| NA | 0 | 1 |
| NA | 1 | 0 |
| NA | 1 | 1 |



| | RAM_ID3 | RAM_ID2 | *RAM_ID1 | *RAM_ID0 | PartNumber - Description |
|--------------------|---------|---------|----------|----------|--|
| Hynix 4GB | 0 | 0 | 0 | 0 | SA00008MN30 (S IC D4 512M16 H5AN8G6NCJR-VKC FBGA ABOI) |
| Micron 4GB | 0 | 0 | 0 | 1 | SA0000ARD60 (S IC D4 8G/2666 MT40A512M16LY-075:E ABOI) |
| Samsung 4GB | 0 | 0 | 1 | 0 | SA000086F30 (S IC D4 512M16 K4A8G165WC-BCTD FBGA 96P) |
| | 0 | 0 | 1 | 1 | |
| No On Board Memory | 1 | 1 | 1 | 1 | No On Board Memory |



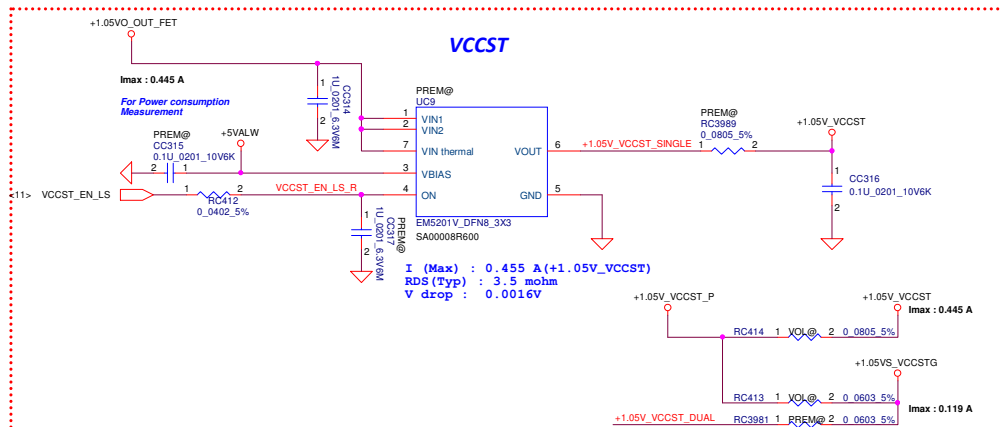
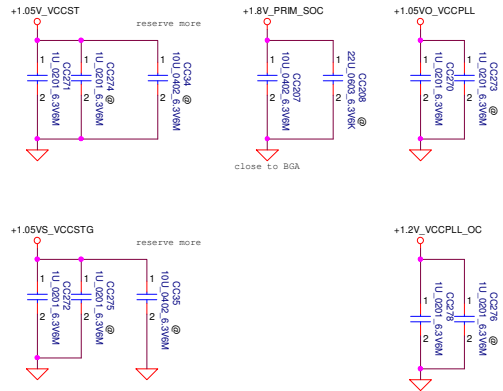
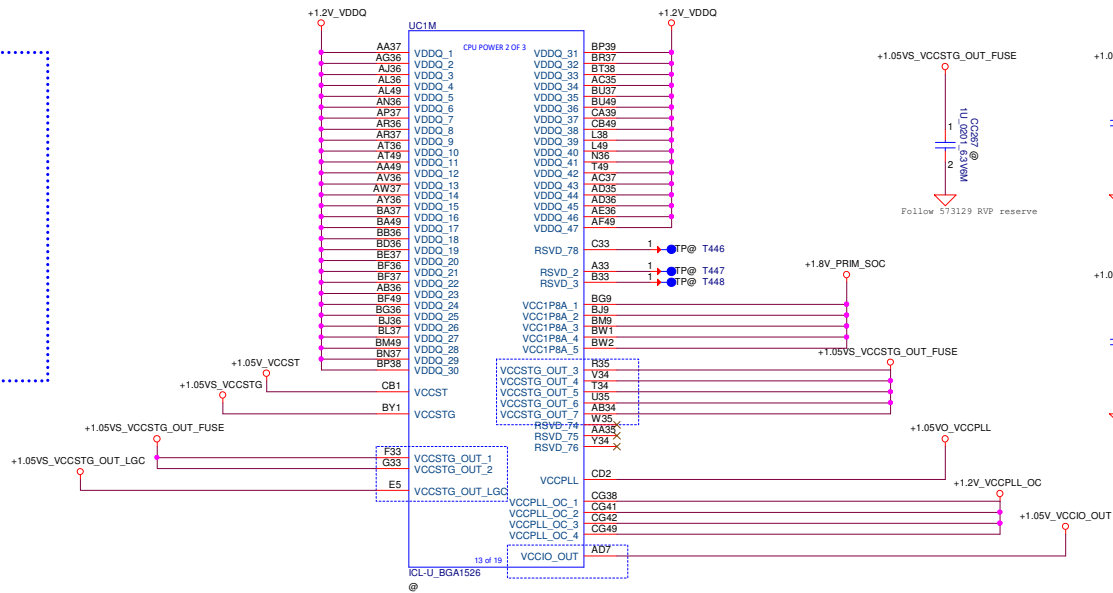
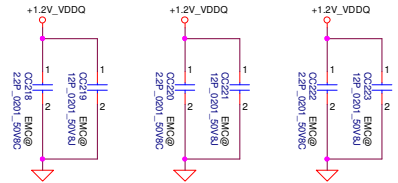
GPP_B23
CPUNSSC CLOCK FREQ
INTERNAL PD 20K
HIGH: 19.2 Mhz (form internal divider)
LOW: 38.4 Mhz (direct form crystal) (Default)

GPP_B18
No Reboot
INTERNAL PD 30K
No Reboot
LOW: Reboot Enable (Default)

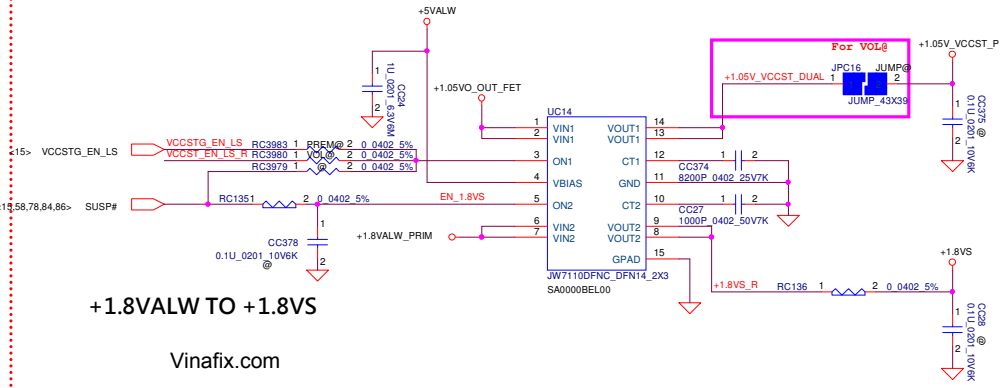
SPKR
TOP SWAP OVERRIDE
INTERNAL PD 20K
HIGH: top-swap-enable
LOW: Disable (Default)

GPP_D16
MFR_MODE_DET_STRAP
Follow 573129_ICL-U_DDR4_SODIMM_RW_SCH_RH_IP0

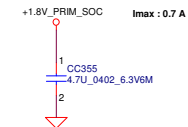

```
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)
```



+1.05V_VCCST (PCH to CPU)



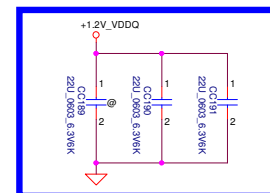
+1.8VALW_PRIM TO +1.8V_PRIM_SOC



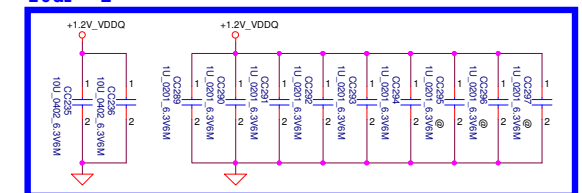
+1.2V_VDDQ TO +1.2V_VCCPLL_OC

Imax : 0.152 A

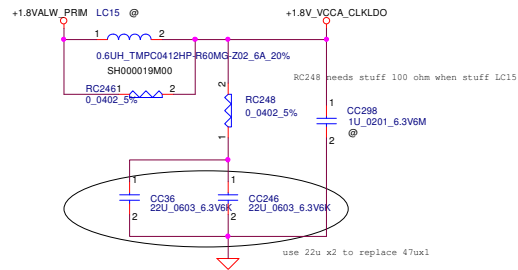
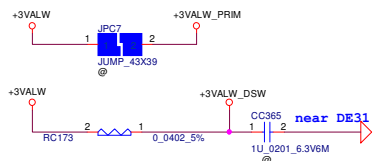
Place on CPU Side
22uF* 2 + 22uF* 1 (Reserved)



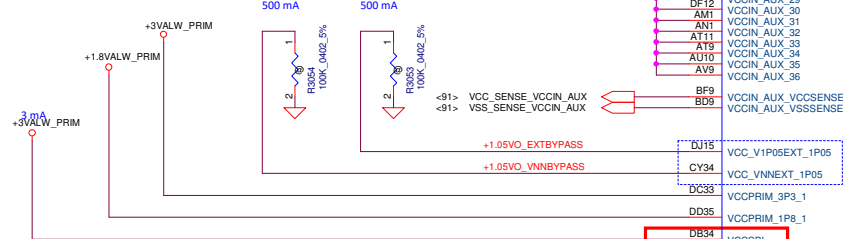
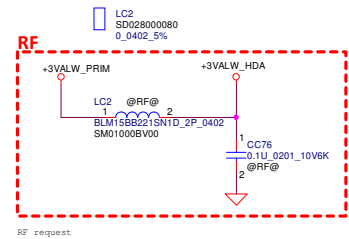
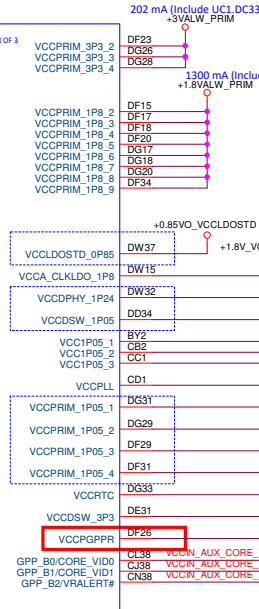
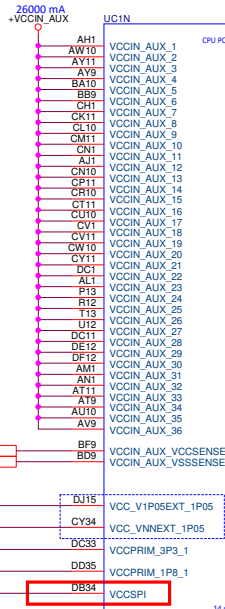
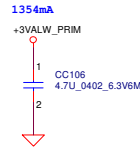
Place on opposite of CPU Side
1uF* 6 + 1uF*3 reserve
10uF* 2



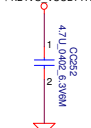
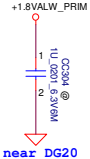
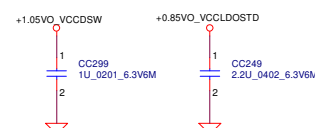
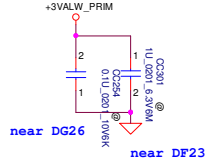
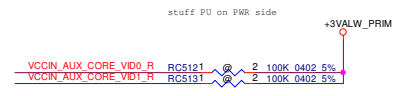
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| | | | | | | Size |
| FH5LI M/B LA-H801P | | | | | | 1.0 |
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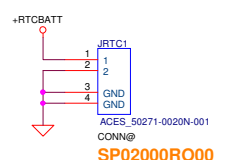
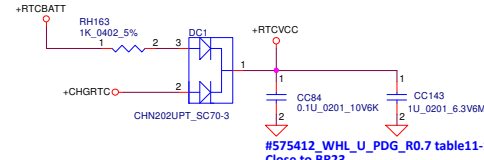
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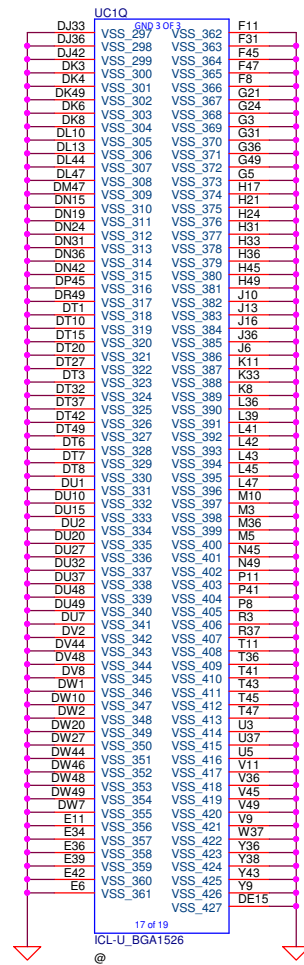
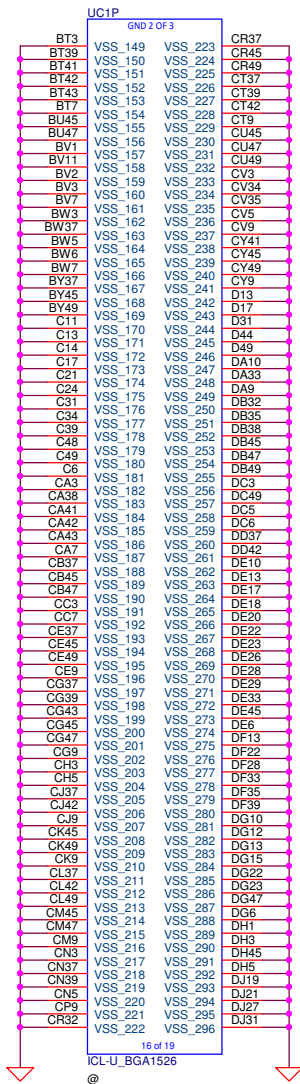
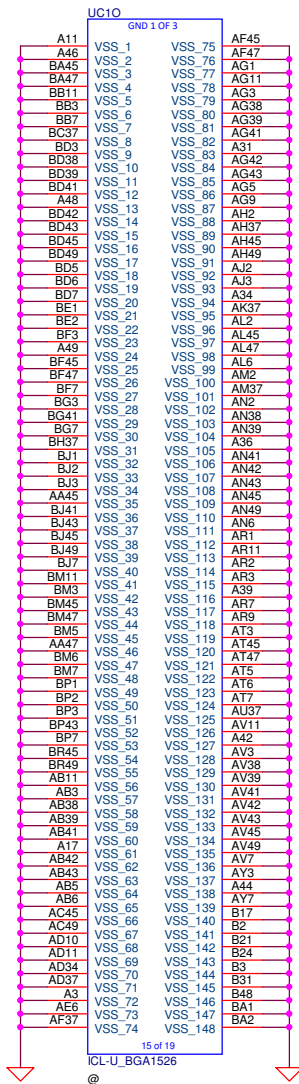
NOTE:
572631_ICL_PCH_LP_EDS_Vol_1_Rev_1p0
VCCGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.
572907_ICL_UY_PDG_Rev1p1
When configured as 3.3V or 1.8V, VCCGPPR can be merged directly with either VCCPRIM_1P8 or VCCPRIM_3P3 depending on their operating voltage.



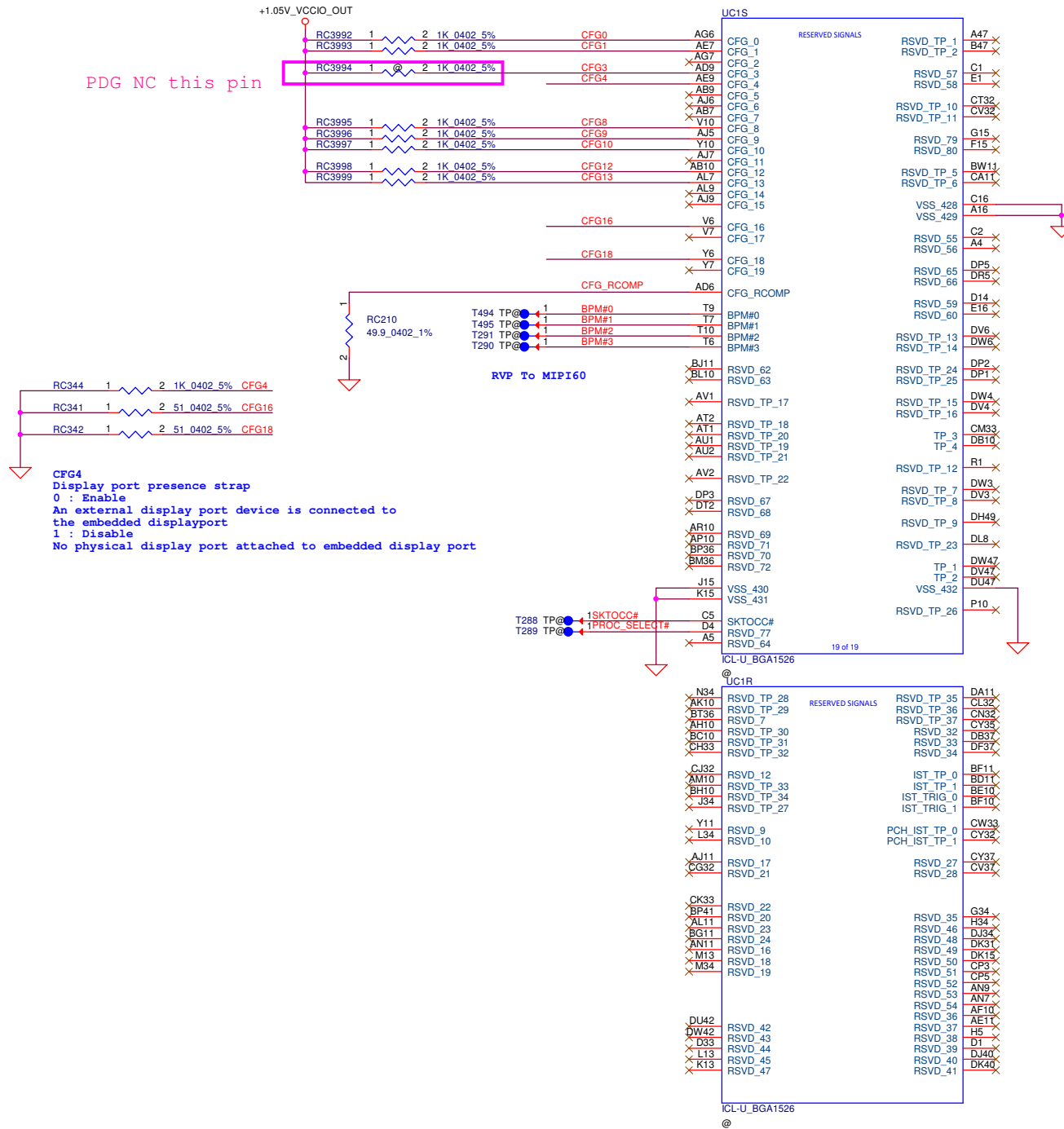
RTC Battery



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PDG NC this pin



5.5.13 CFG Signals Functionality and Termination

Table 5-76. CFG Signals Functionality and Termination

| CFG | Description | Termination | Resistor |
|-----------------------|---|----------------|----------|
| CFG0 | CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. | Pull Up | 1K Ohm |
| CFG1,8,9,10,12,13 | RSVD | Pull Up | 1K Ohm |
| CFG2,3,5,6,7,11,14,15 | RSVD | No termination | N/A |
| CFG4 | CFG[4]: eDP enable: — 1 = Disabled. — 0 = Enabled. | Pull Down | 1K Ohm |

Note: Refer Chapter 13, "Platform Debug and Test Hooks" for debug connectivity guidelines.

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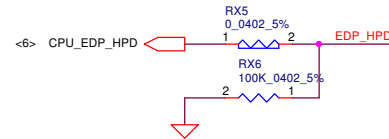
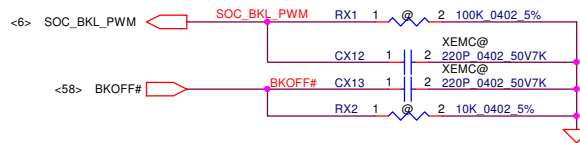
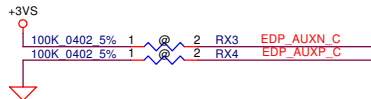
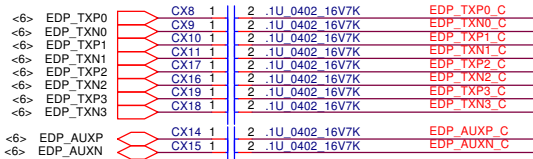
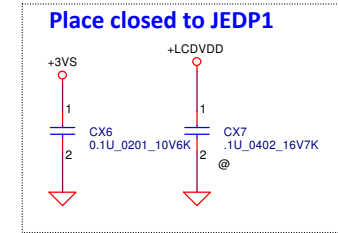
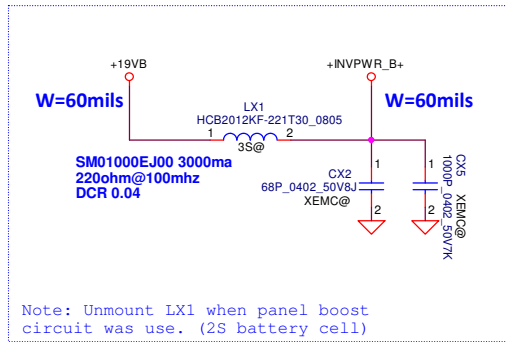
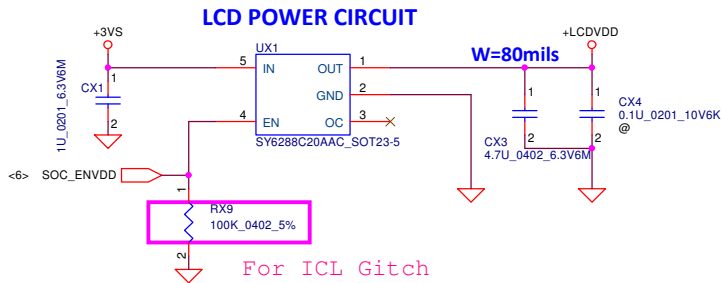
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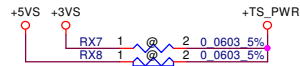
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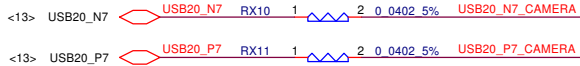
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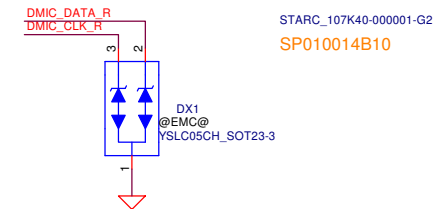
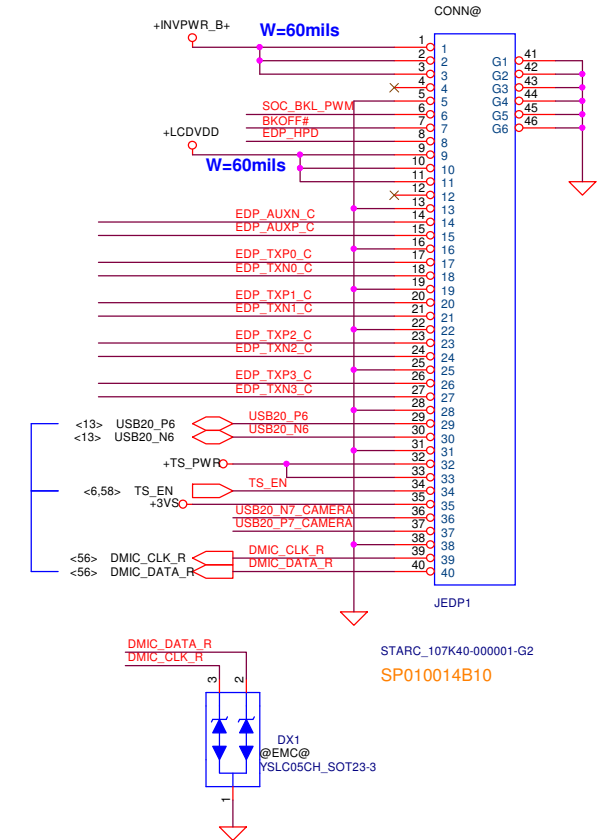
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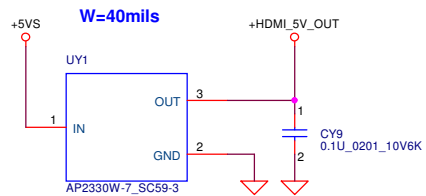
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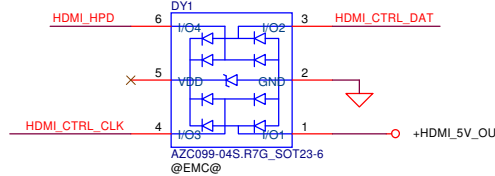
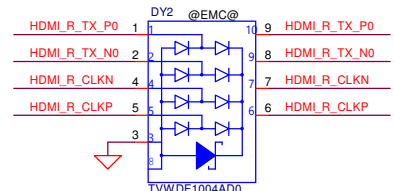
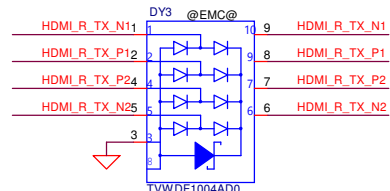
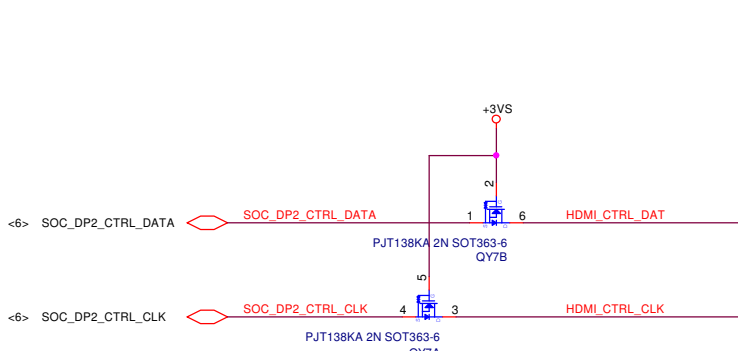
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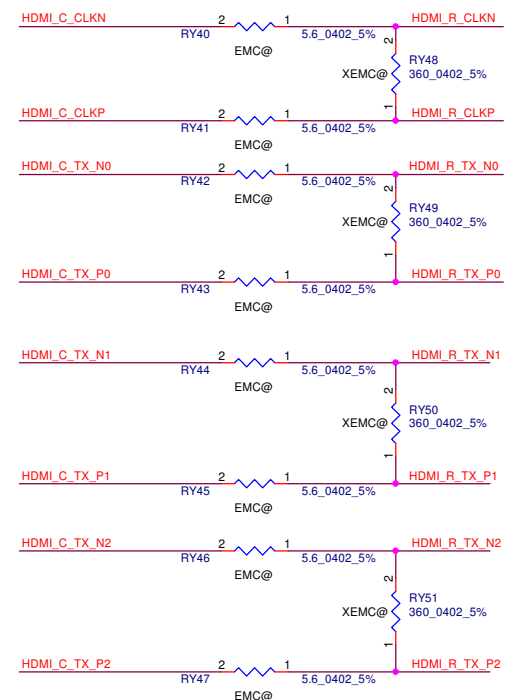
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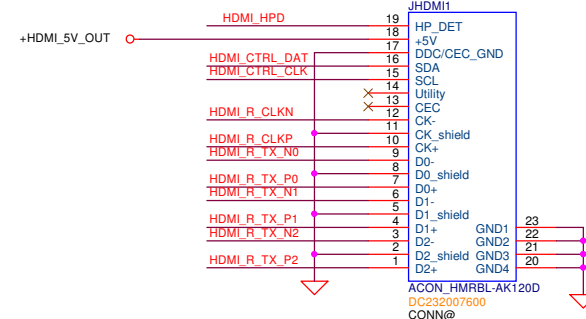
port 0, 2 swap for INTEL HDMI



P/N: SC300001G00,S DIO(BR) AZC099-04S.R7G SOT23 ESD



HDMI connector



SYMBOL: DC232004700

Vinafix.com

| | | | | | |
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| | | | | Date: Tuesday, October 15, 2019 | Rev 1.0 |
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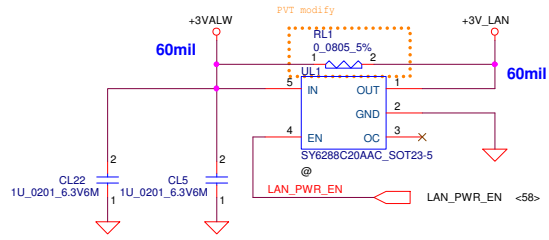
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| | | | | Date: Tuesday, October 15, 2019 | Rev 1.0 |
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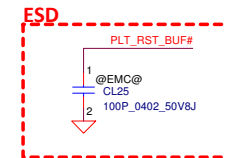
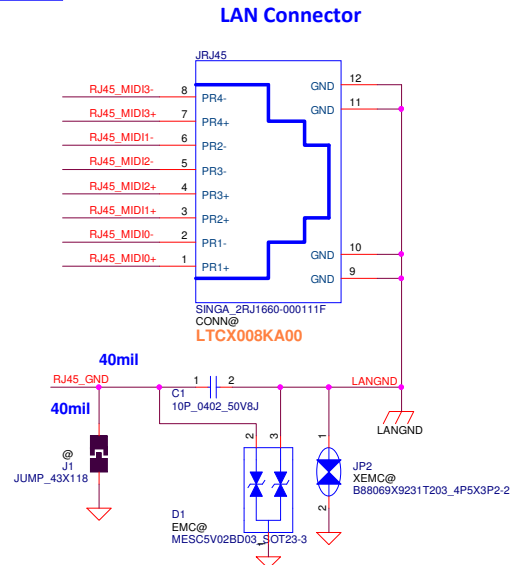
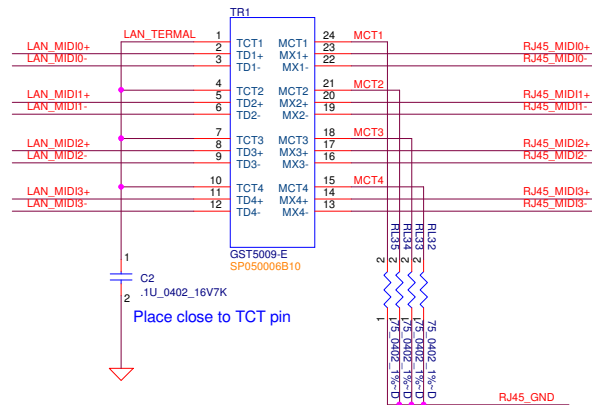
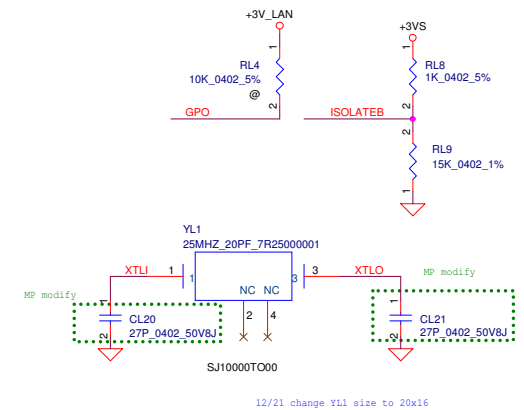
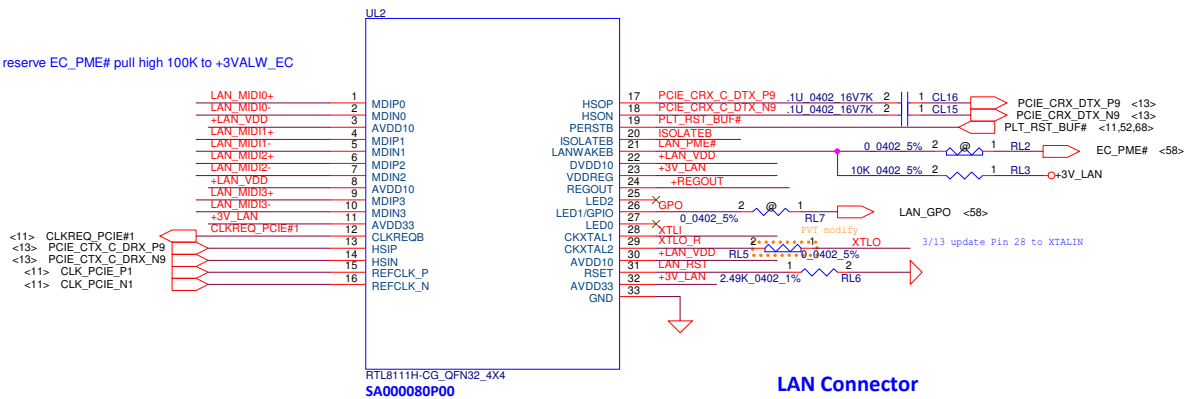
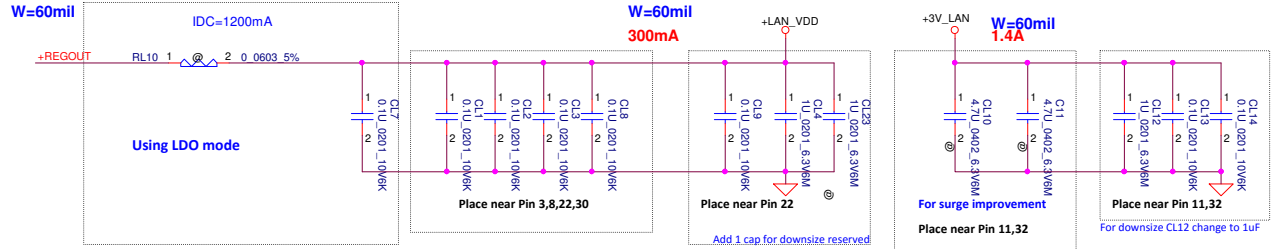
LAN-RTL811H



From EC

High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

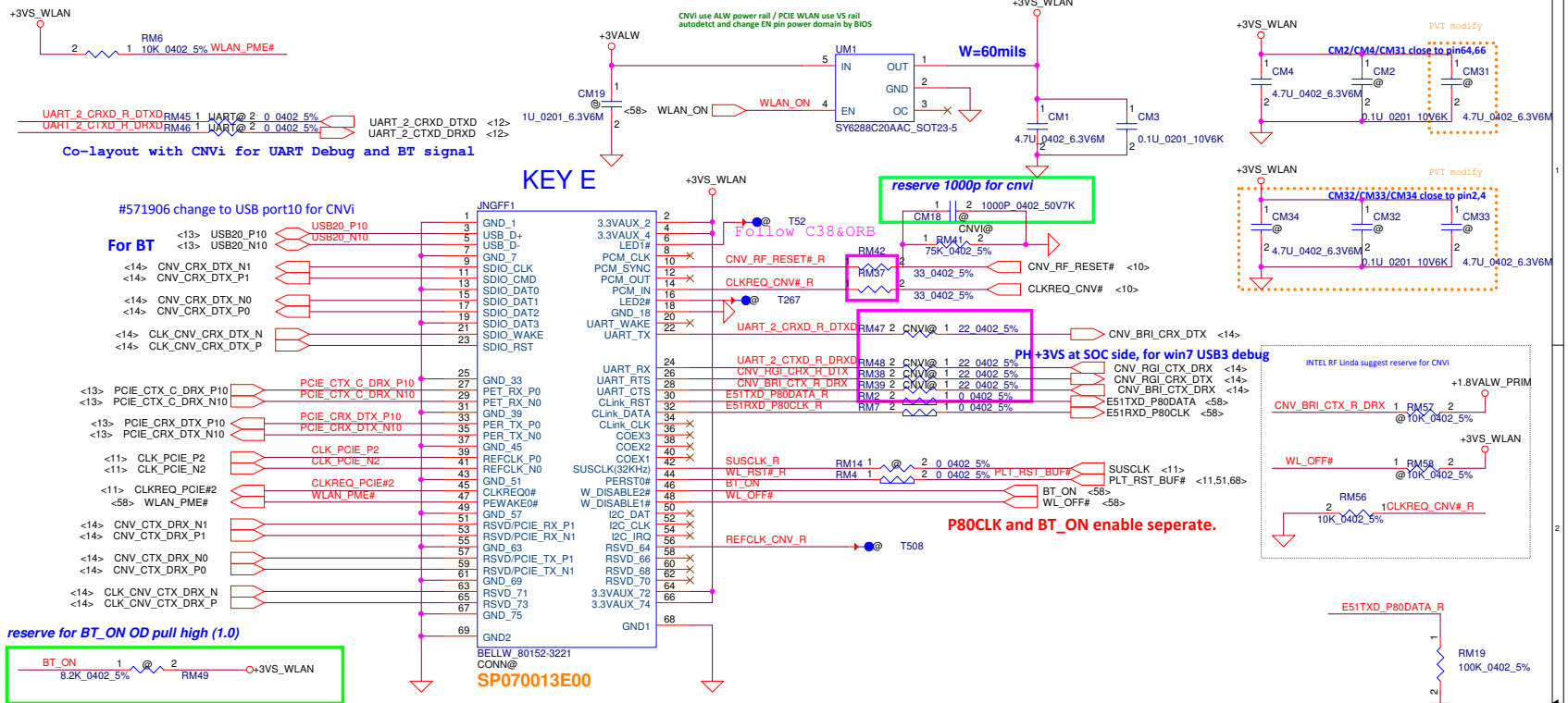
+3V_LAN Rising time must >0.5ms and <100ms



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NGFF WL+BT (KEY E)

| | | | |
|----|-----------------------------------|--------------------------|----|
| 74 | 2.3V | GND | 75 |
| 75 | 2.3V | RESERVED[REFCLK1] | 76 |
| 76 | UMM_Power_SMC[IO]PwMn12 | RESERVED[REFCLK1] | 77 |
| 68 | UMM_Power_SMC[REQREQ] | Reserved[Dir1] | 67 |
| 66 | UMM_SVP[PERST2] | Reserved[Dir2] | 65 |
| 64 | RESERVED | Reserved[Per1] | 61 |
| 62 | ALERT# [IO(0/3)] | Reserved[Per2] | 59 |
| 60 | QC CLK (IO(0/3)) | Reserved[Per3] | 58 |
| 58 | QC DATA (IO(0/3)) | GND | 57 |
| 56 | WIDABLE[LE1] (IO(0/3/V)) | REFCLK[IO(0/3/V)] | 55 |
| 54 | Reserved_WIDABLE[LE2] (IO(0/3/V)) | CARCLK[IO(0/3/V)] | 53 |
| 52 | PERST2P (IO(0/3/V)) | GND | 51 |
| 50 | SUSC1[CRASH] (IO(0/3/V)) | REFCLK[IO] | 49 |
| 48 | CCD1 [IO(0/1/V)] | REFCLK[IO] | 46 |
| 46 | CCD0[IO(0/1/V)] | REFCLK[IO] | 45 |
| 44 | CCD0B[IO(0/2/V)] | REFCLK | 43 |
| 42 | VENDOR DEFINED | REFCLK | 40 |
| 40 | VENDOR DEFINED | REFCLK | 39 |
| 38 | VENDOR DEFINED | REFCLK | 37 |
| 36 | UART KTS (IO(0/1/V)) | REFCLK | 35 |
| 34 | UART CTS (IO(0/1/V)) | REFCLK | 33 |
| 32 | UART TX (IO(0/1/V)) | | |
| 22 | UART Rx (IO(0/1/V)) | SIO Reserved (IO(0/1/V)) | 23 |
| 20 | UART WAKEUP (IO(0/3/V)) | SIO WAKEUP (IO(0/1/V)) | 21 |
| 18 | GND | SIO DATA TX (IO(0/1/V)) | 19 |
| 16 | UDAP2 (IO) | SIO DATA TX (IO(0/1/V)) | 17 |
| 14 | PCM_OUT[IO]S_SO_OUT[IO(0/1/V)] | SIO DATA TX (IO(0/1/V)) | 15 |
| 12 | PCM_IN[IO]S_SO_IN[IO(0/1/V)] | SIO DATA TX (IO(0/1/V)) | 13 |
| 10 | PCM_SYNC[IO]S_SO[IO(0/1/V)] | SIO DATA TX (IO(0/1/V)) | 11 |
| 8 | PCM_CLK[IO]S_SO[IO(0/1/V)] | SIO CLK[IO(0/1/V)] | 9 |
| 6 | UDAP1 (IO) | GND | 7 |
| 4 | 2.5V | USB_DP | 5 |
| 2 | 0.5V | USB_DP | 3 |



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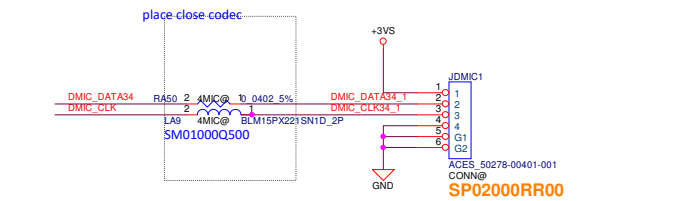
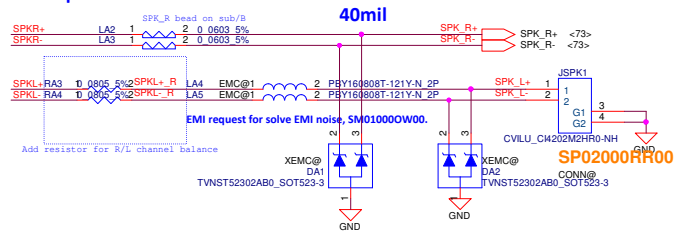
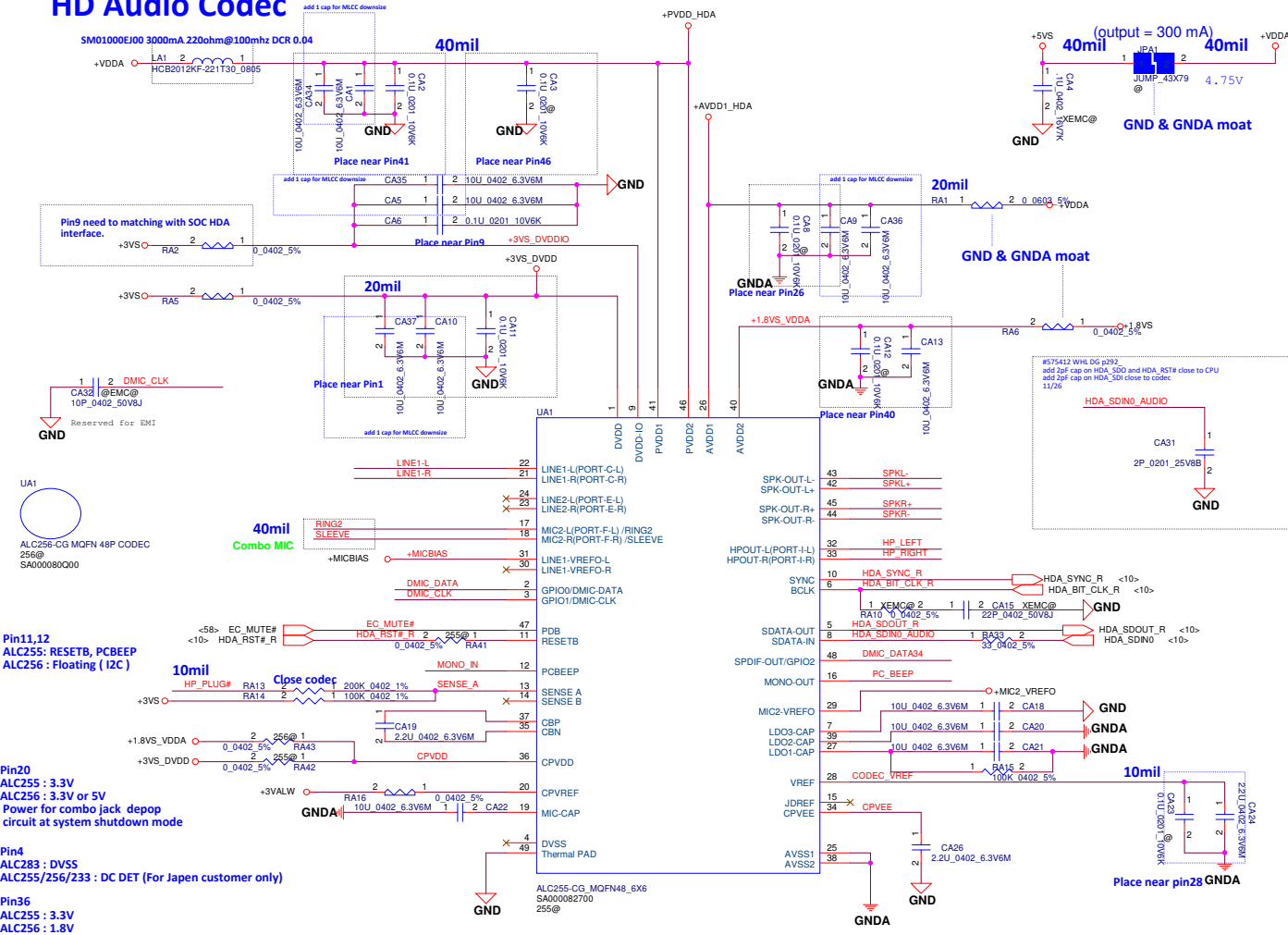
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| | | | | Date: Tuesday, October 15, 2019 | Rev 1.0 |
| | | | | Sheet 54 of 102 | |

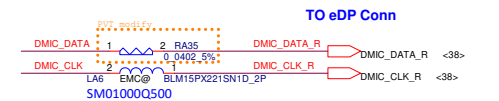
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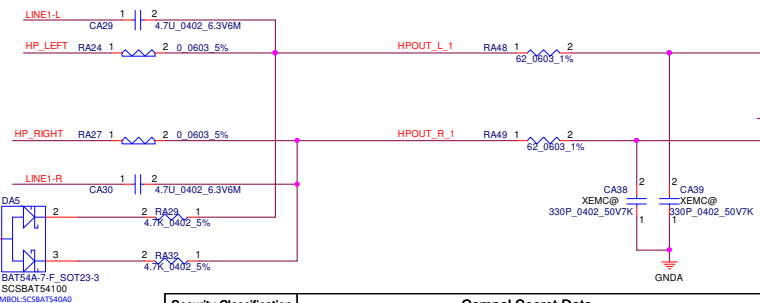
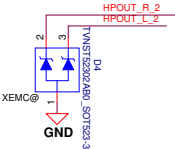
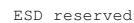
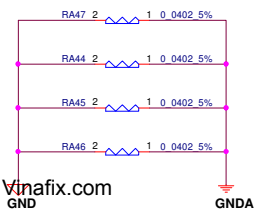
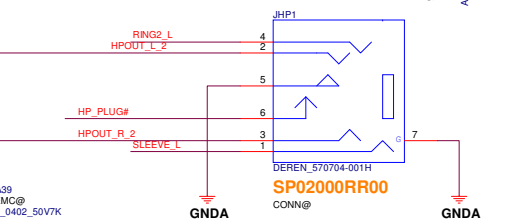
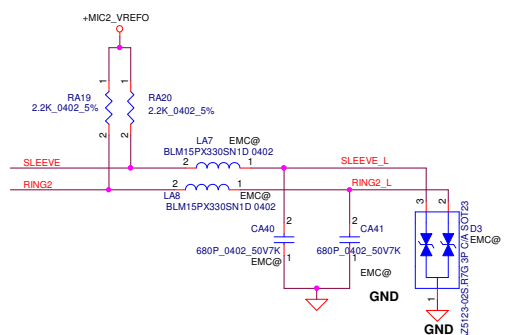
HD Audio Codec



Digital MIC



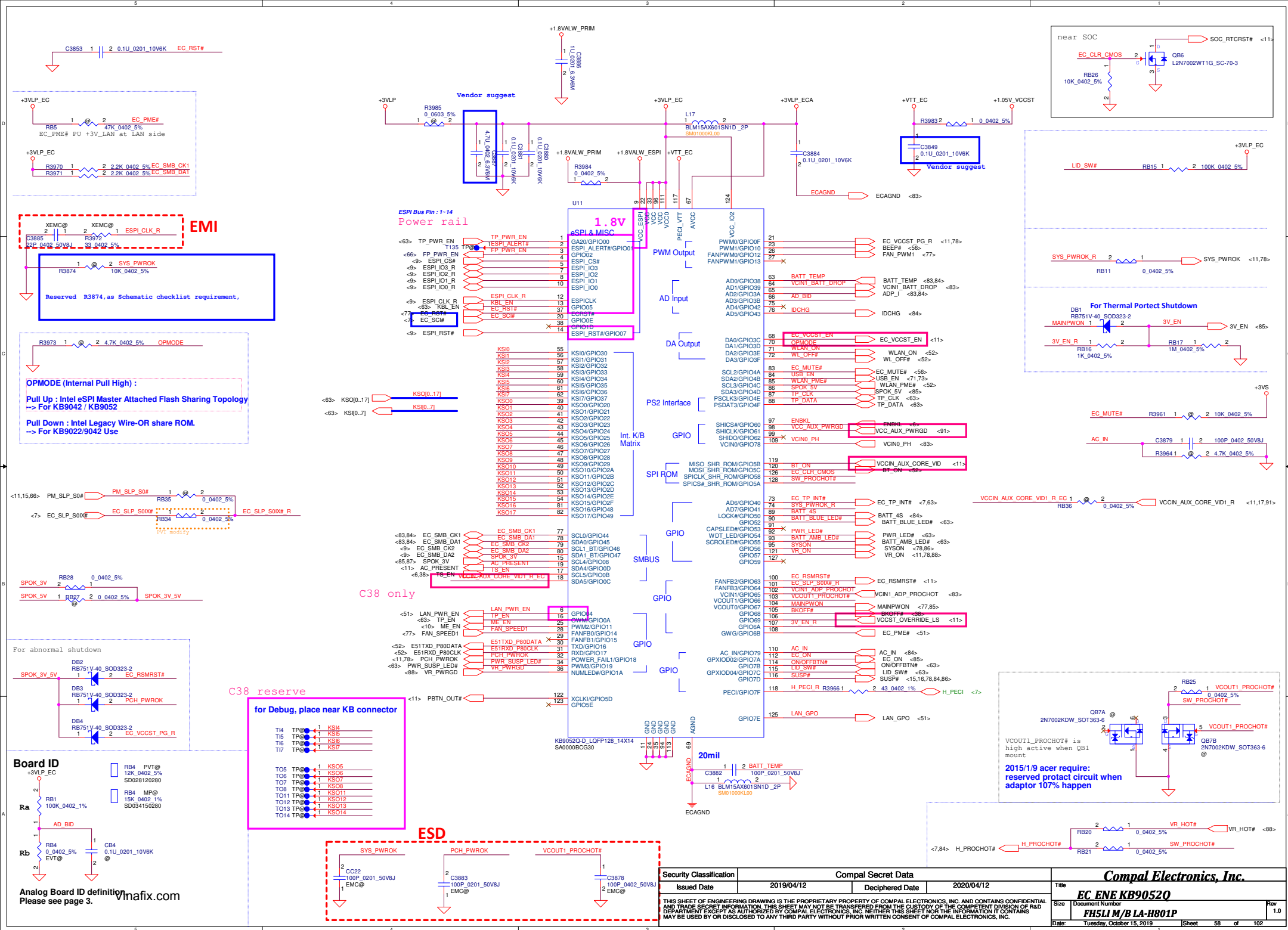
Headphone Out



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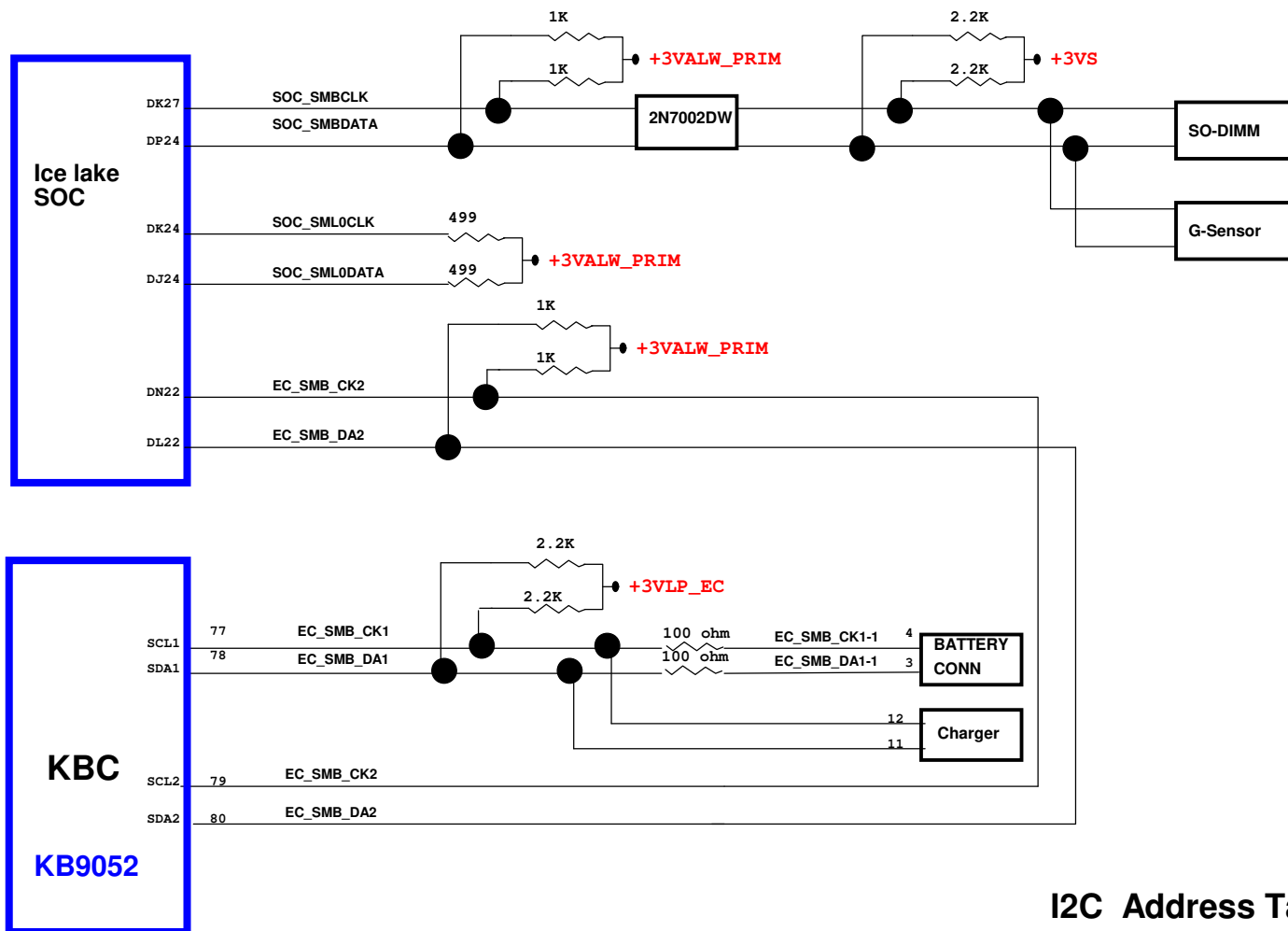


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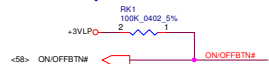
I2C Address Table

| BUS | Device | Address (8 bit) |
|--------------------------|-----------------------|-----------------|
| I2C_1 (+3VALW_PRIM) | TM-P3393-003 (TP) | 0x2C |
| | FA577E-1206 (TP-ELAN) | 0x15 |
| | SA577C-12A0 (TP-ELAN) | 0x15 |
| SOC_SMBCLK (+3VS) | SO-DIMM1 | TBD |
| | G-Sensor | 0x30 |
| EC_SMB_CK2 (+3VALW_PRIM) | SOC | 0x90 |
| | | |
| EC_SMB_CK1 (+3VLP) | BQ24781 (Charger IC) | 0x12 |
| | BATTERY PACK | 0x16 |

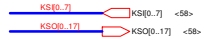
Reserve Page

| | | | | | |
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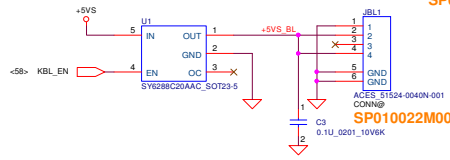
ON/OFF BTN



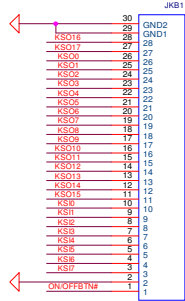
DVT: remove SWK1 switch button



KB BackLight

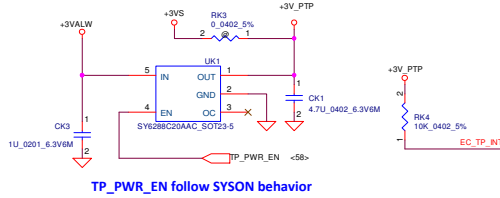


KB Conn.

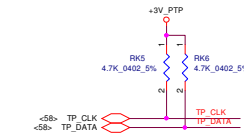
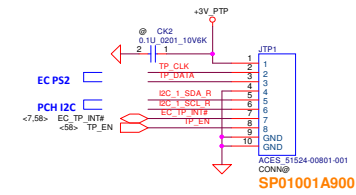
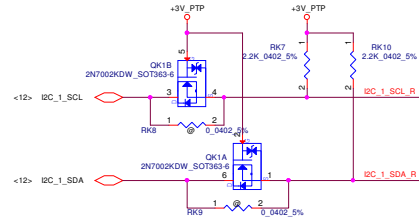


ACES_85201-2805
CONN@
SP01000GO00

TP/B Conn.

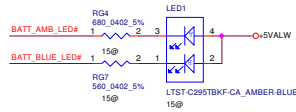


TP_PWR_EN follow SYSON behavior

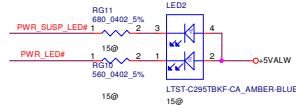


LED for 15" UMA

Battery LED



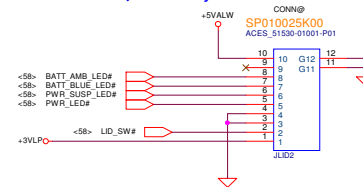
Power LED



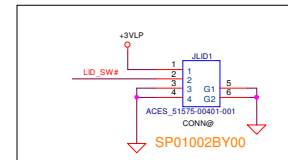
LID for 15" DIS

MB LID SW remove on UMA SKU

LID/B with LED for 17" UMA & DIS



LID/B for 15" UMA 4pin



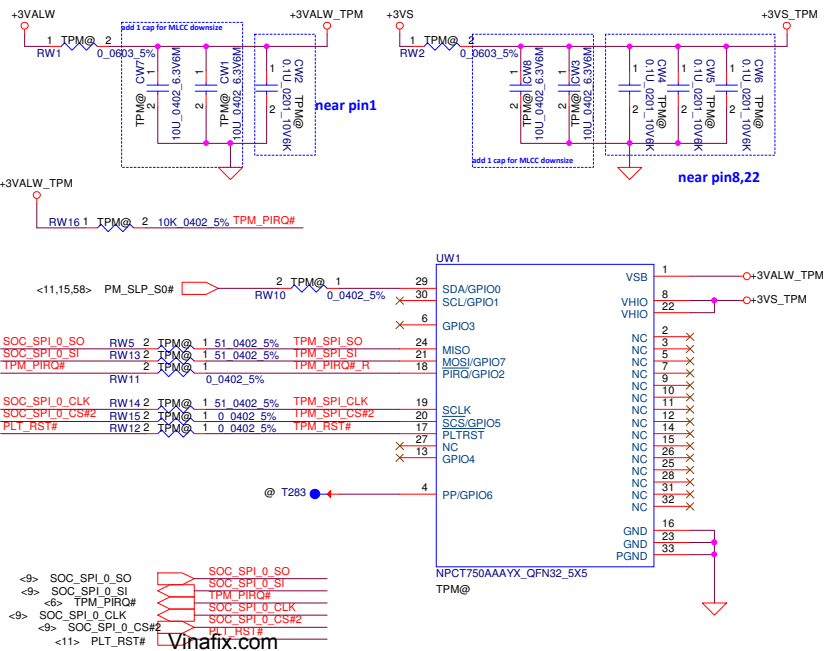
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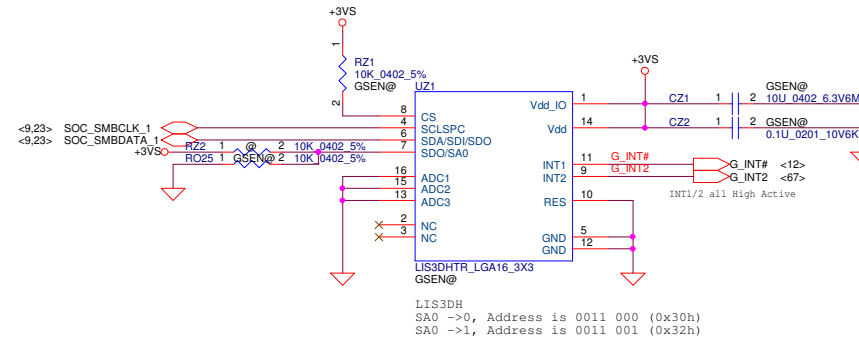
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|---|------------|--------------------|------------|---------------------------------|---------------------------------------|
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TPM 2.0



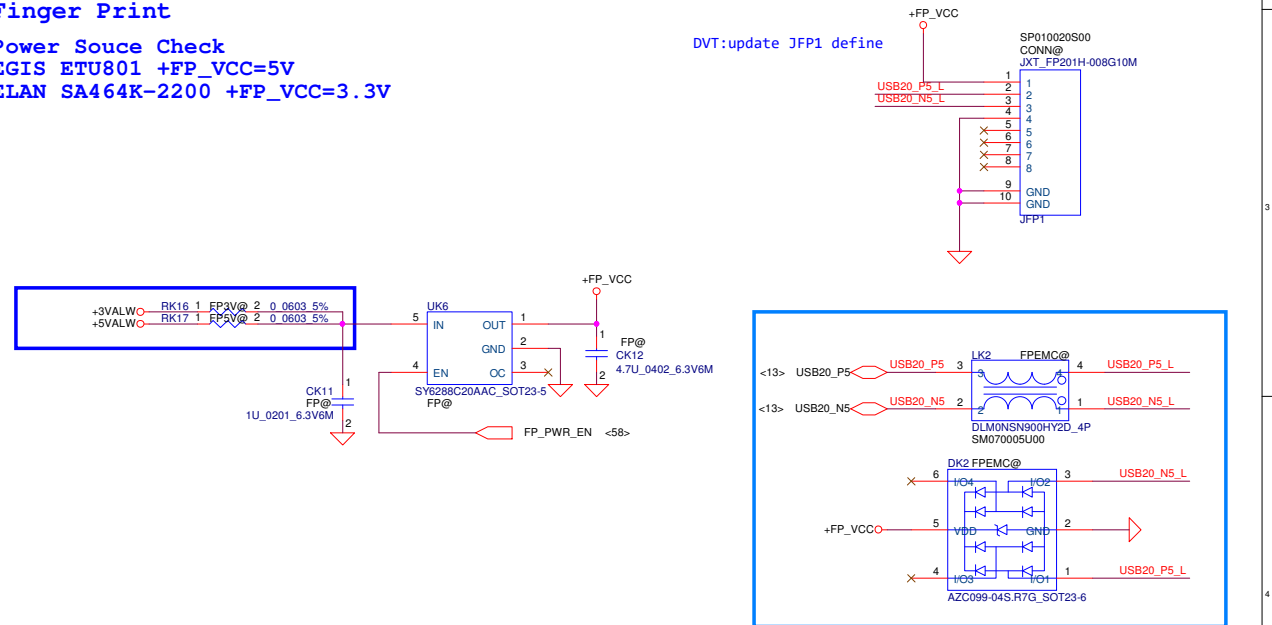
SA0000AQ230, S IC NPCT750AAAYX QFN 32P TPM (SPI interface)

G-Sensor reserved for BA serial

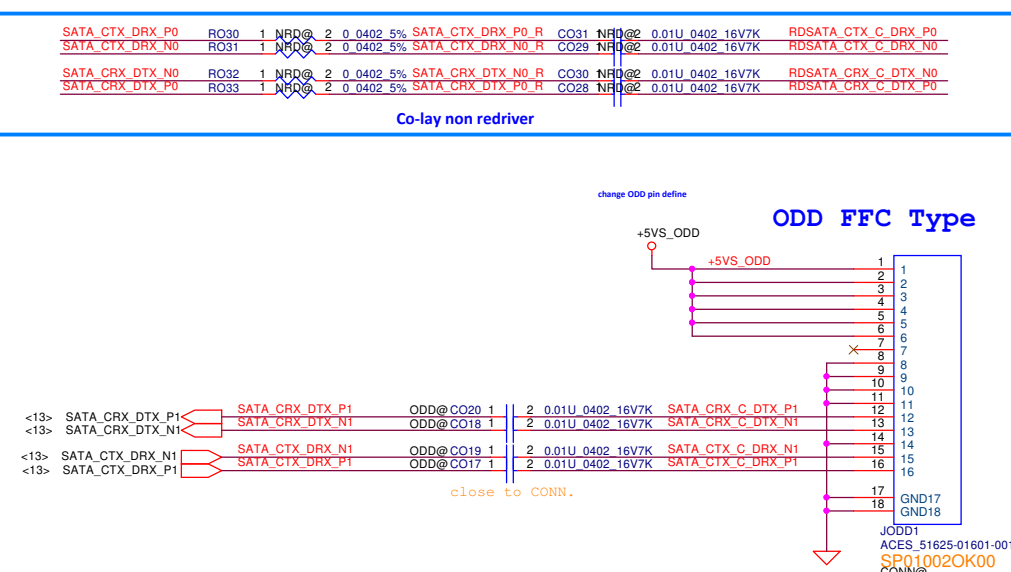
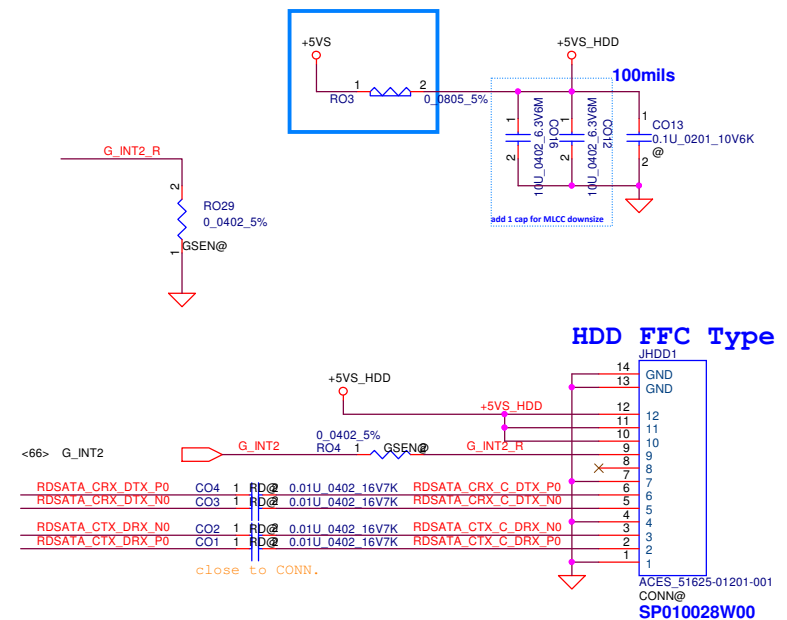
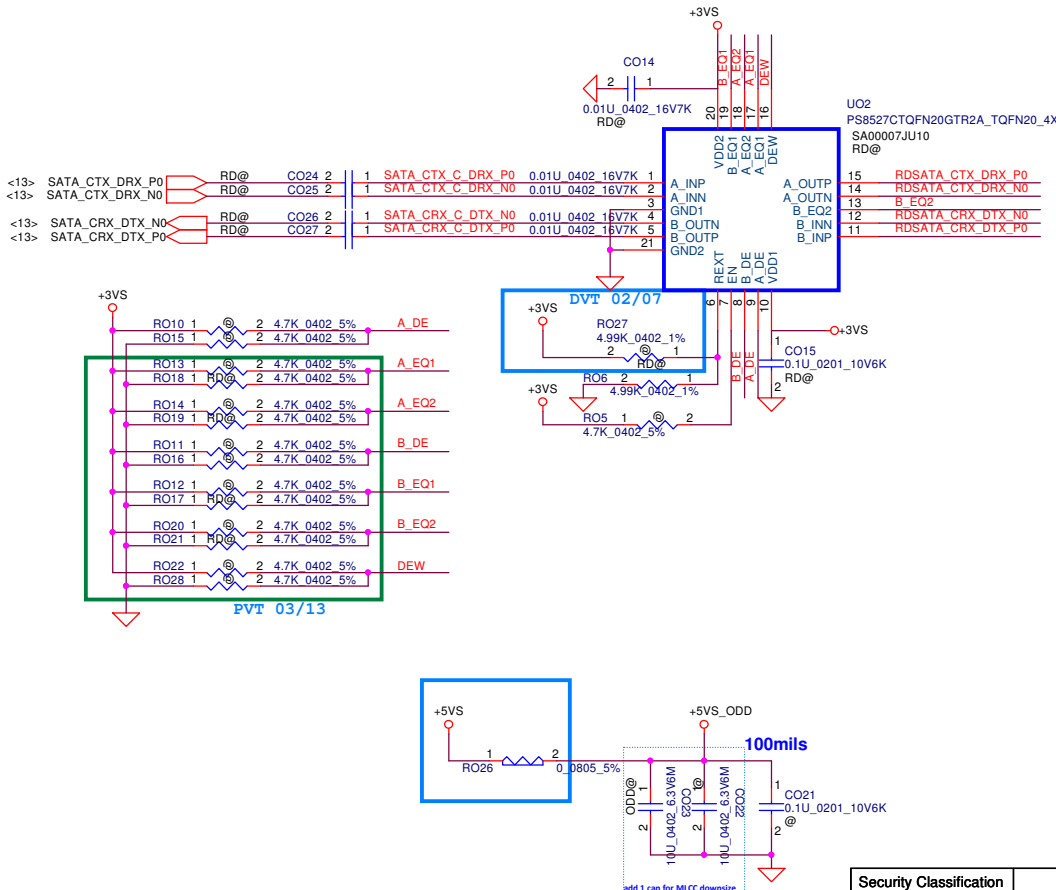


Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



| | | | | | |
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| | | | | | | | | Document Number | | | |
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KEY M

| | |
|---------------|----|
| PETp0/SATA-A+ | 49 |
| PETn0/SATA-A- | 47 |
| GND | 45 |
| PERp0/SATA-B- | 43 |
| PERn0/SATA-B+ | 41 |

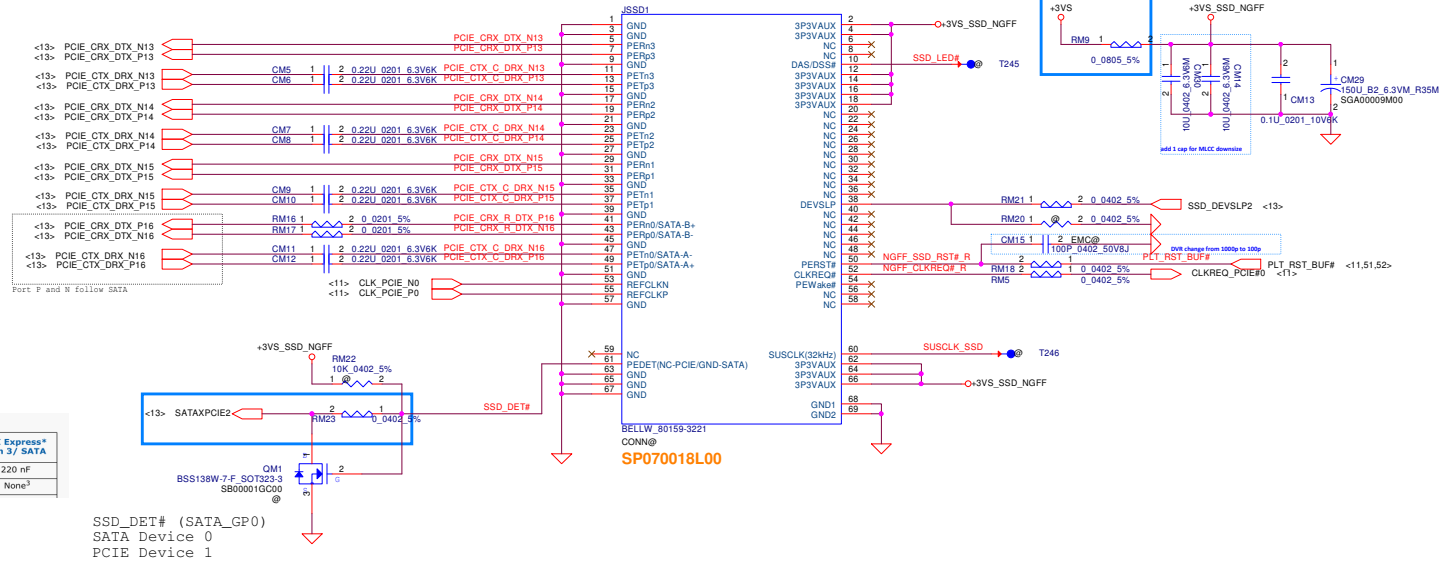


Table 6-26. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

| Condition | PCI Express* Gen 2 Only | PCI Express* Gen 3 Only | SATA Only | PCI Express* Gen 2/ SATA | PCI Express* Gen 3/ SATA |
|--------------|----------------------------|----------------------------|--------------------|-----------------------------|-----------------------------|
| Processor Tx | 100 nF | 220 nF | 10 nF | 100 nF | 220 nF |
| Processor Rx | None | None | 10 nF ¹ | None ² | None ³ |

```
SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1
```

| | | | | | |
|---|------------|--------------------|------------|--------------------------|---------------------------|
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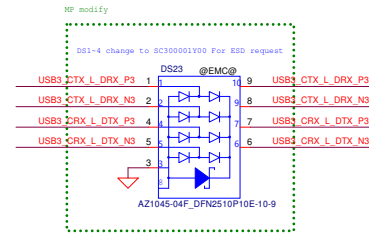
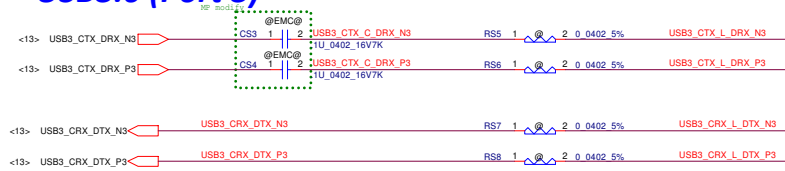
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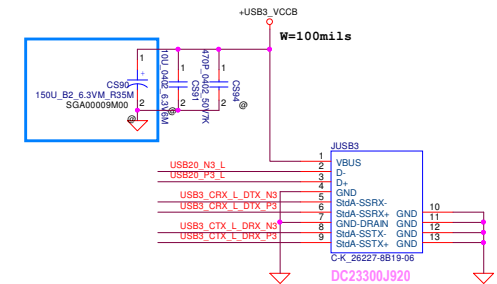
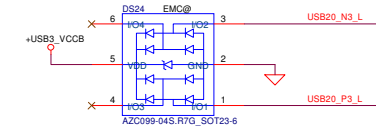
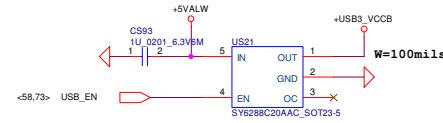
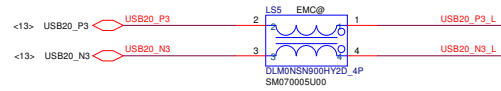
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USB3.0 (Port 3)

USB3 port reserved

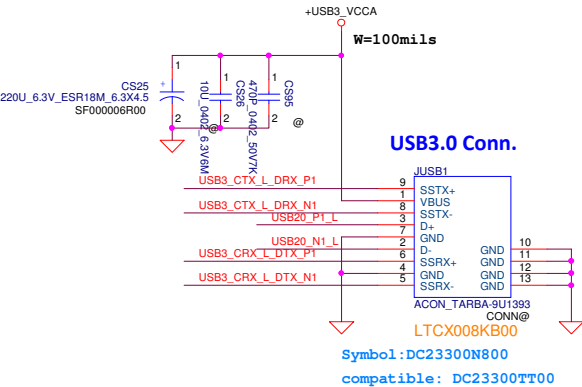
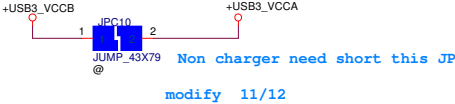
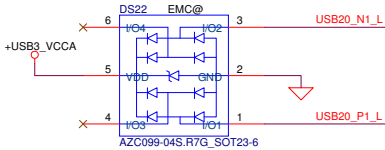
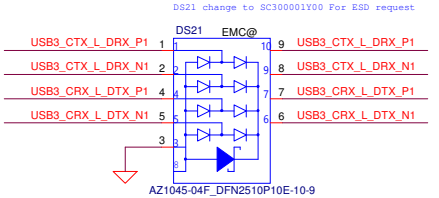
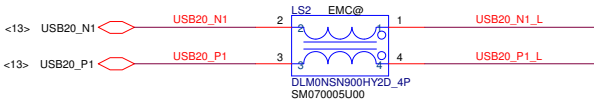
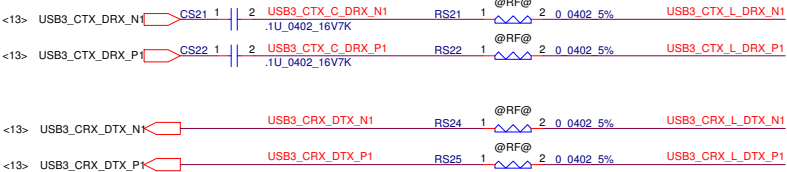


USB2.0 (Port 3)



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USB3.0 (Port 1)



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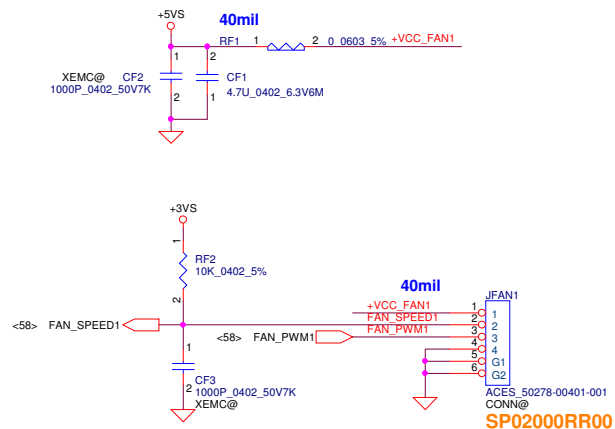
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| | | Tuesday, October 15, 2019 | | 1.0 | |
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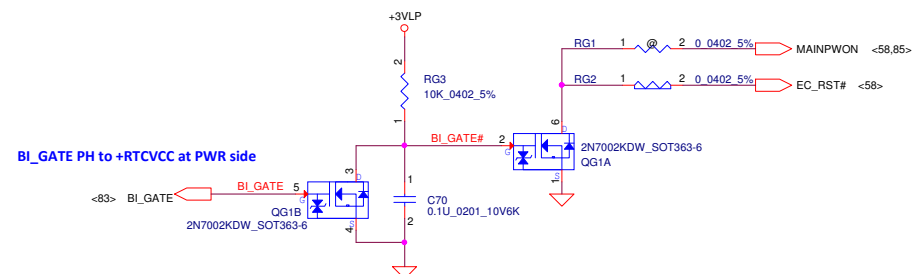
FAN1 Conn



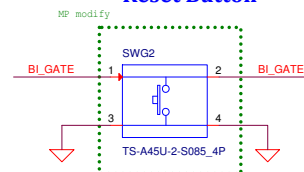
Screw Hole



Reset Circuit

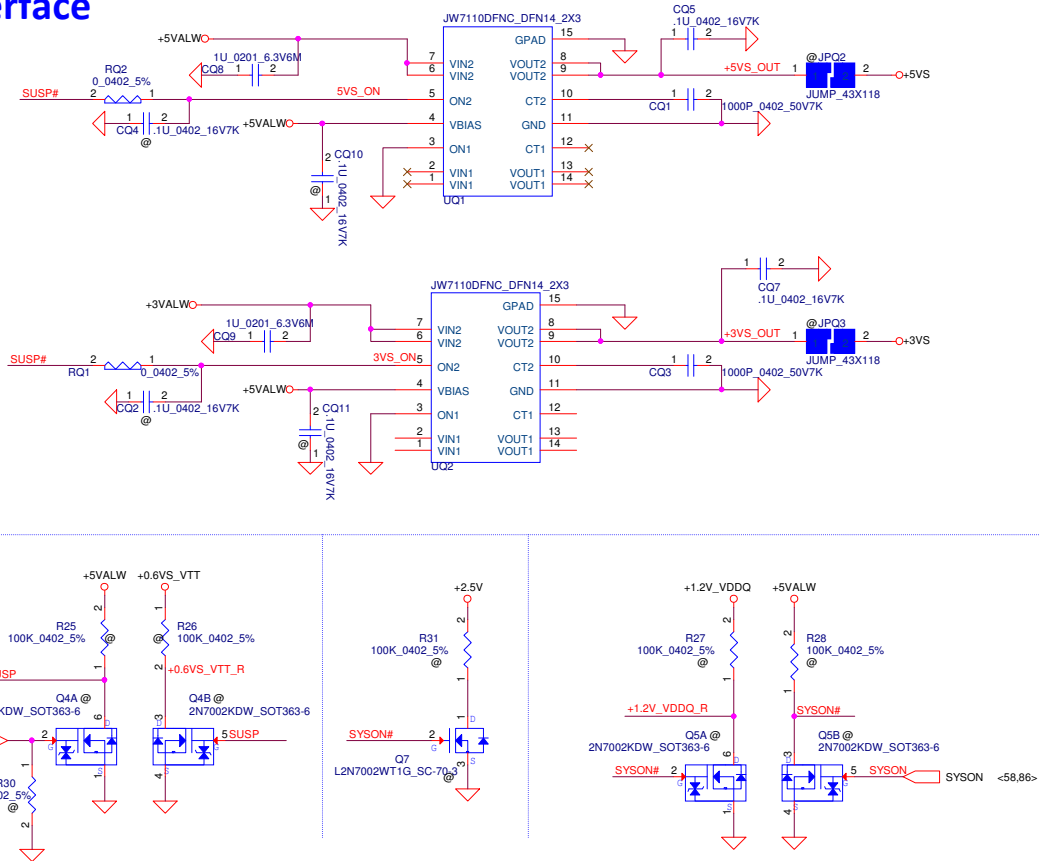


Reset Button

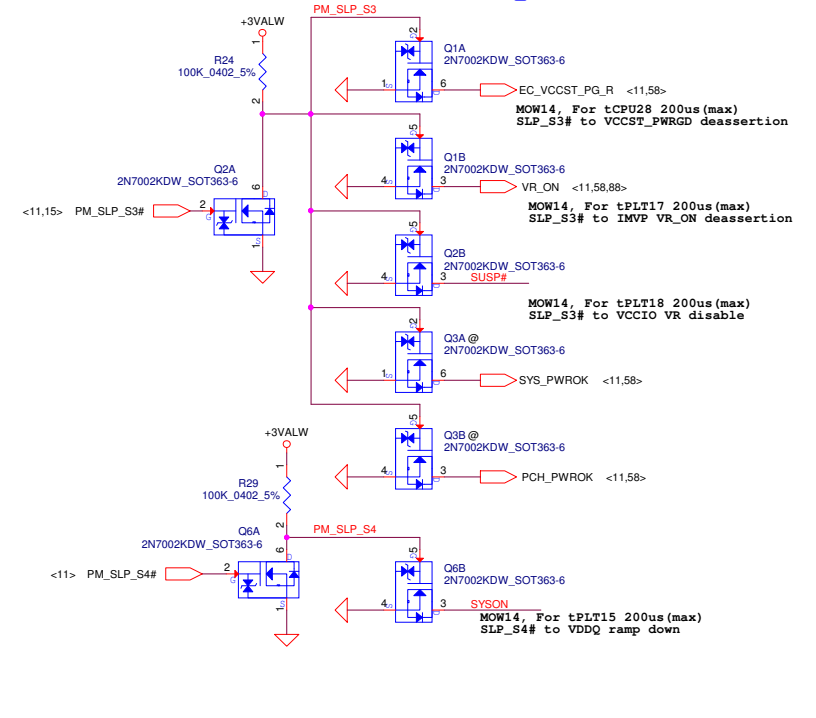


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|---|--------------------|-----------------|------------|--------------------------|-----------------------------|--------|
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| | | | | Date | Wednesday, October 30, 2019 | |
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DC Interface



For Power ON/Off Sequence



Reserve Page

| | | | | | |
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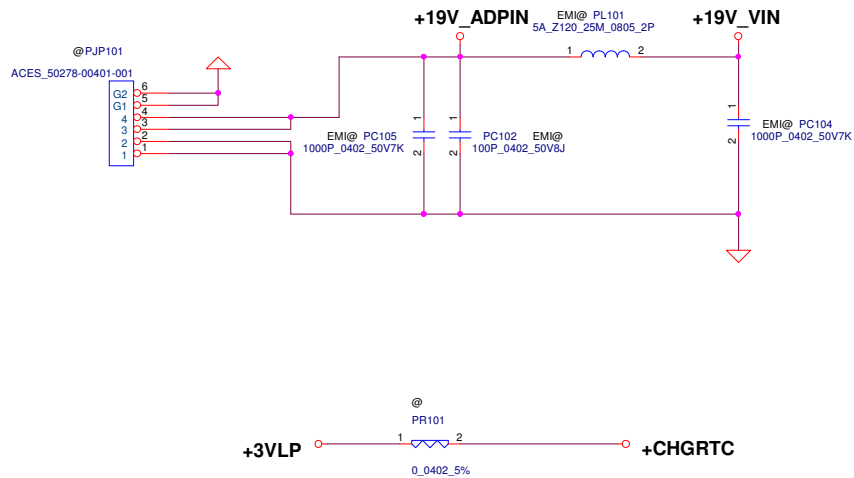
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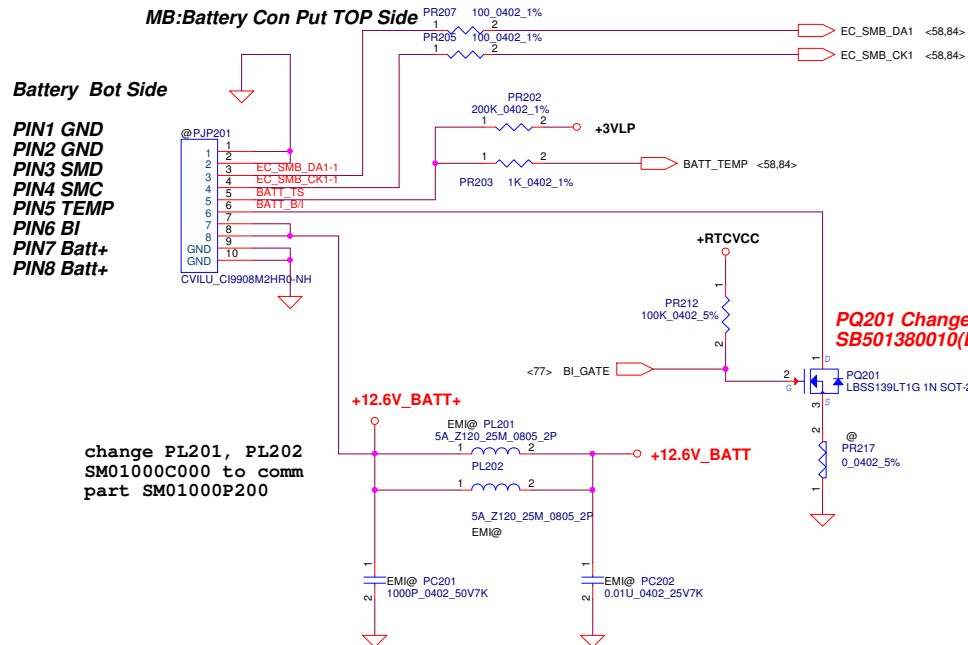
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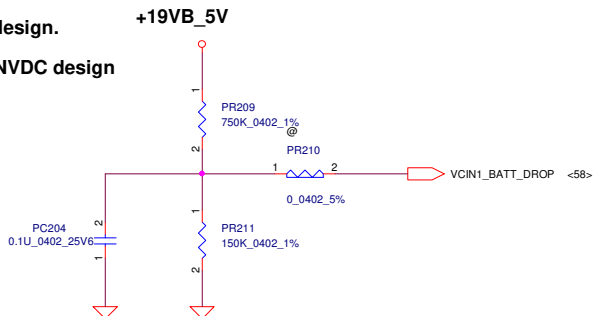
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2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

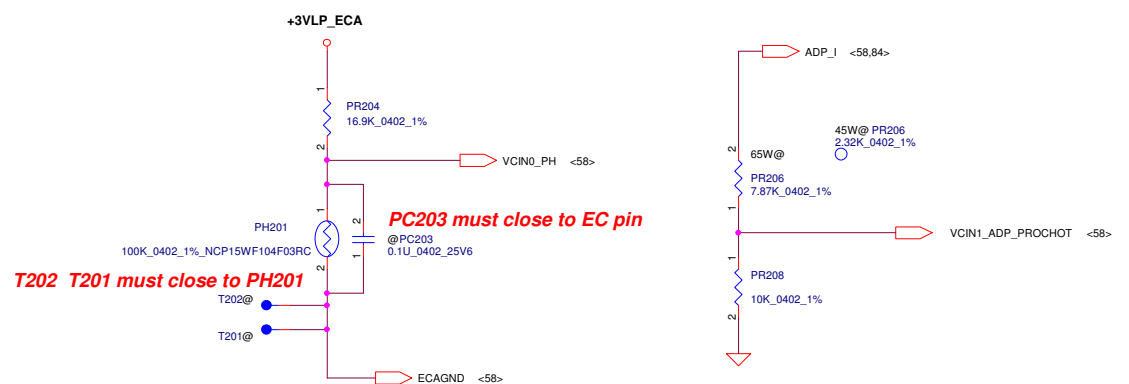
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50K if Battery is 2-cell NVDC design
B+=6V

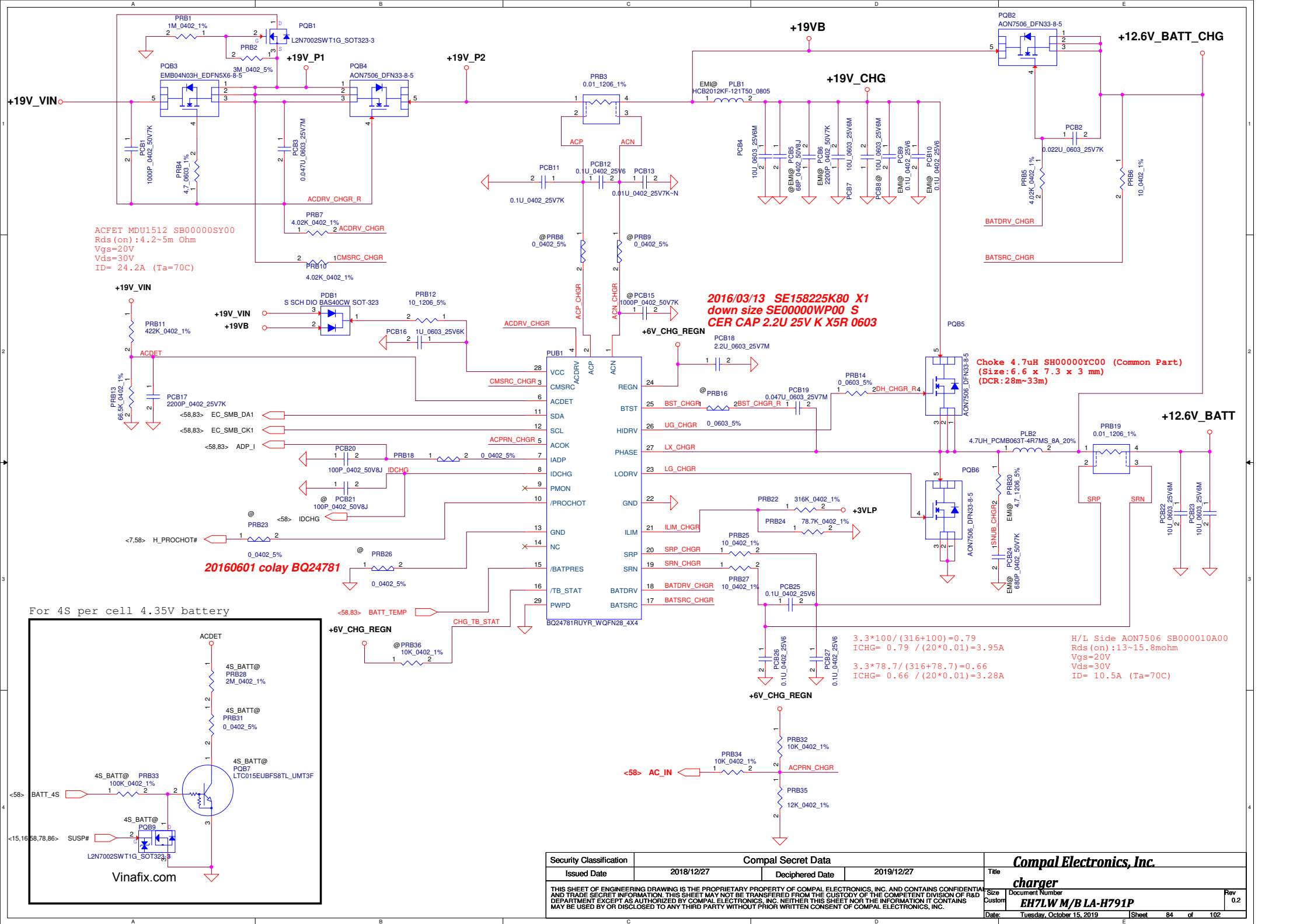


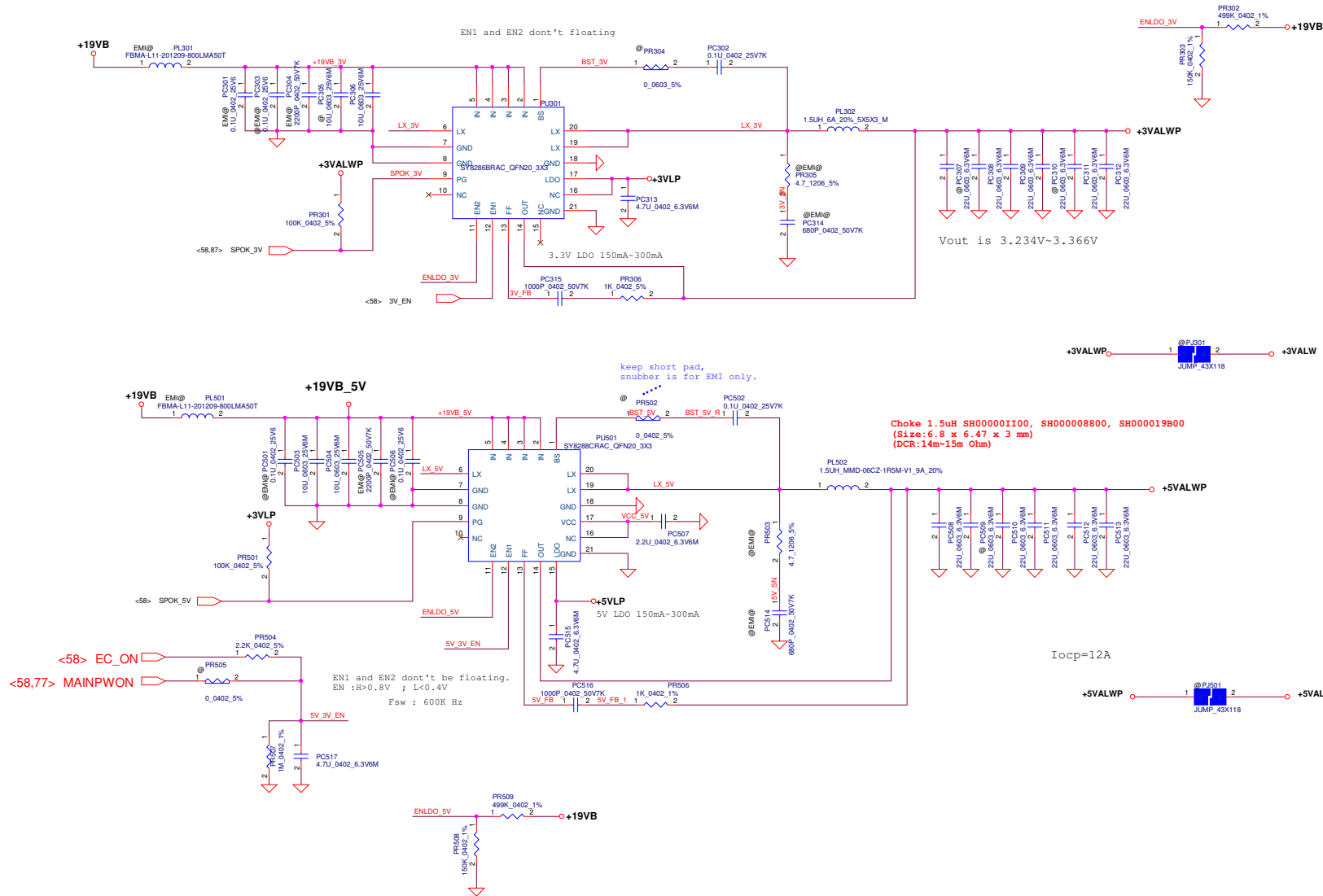
2016/11/16 update

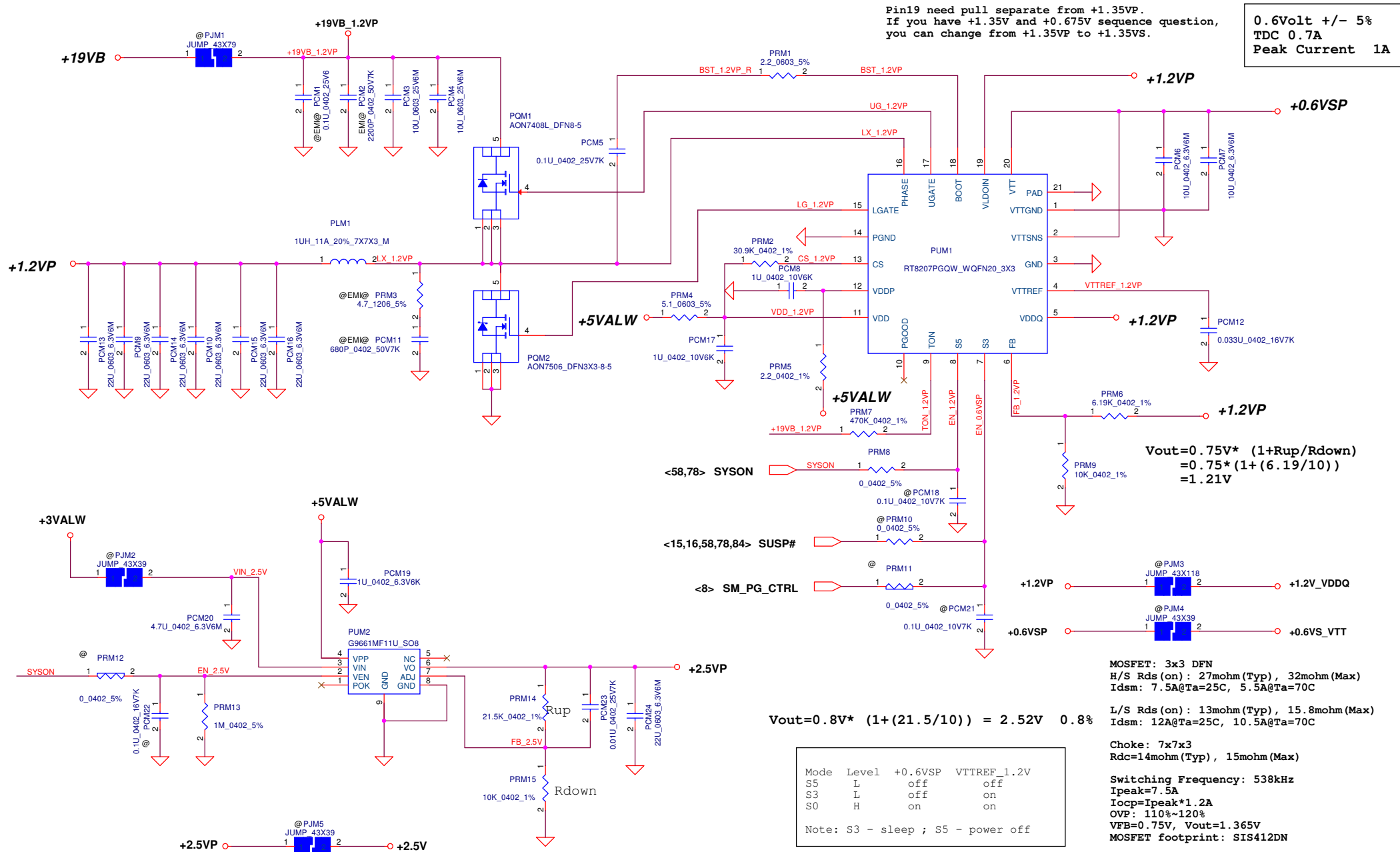
| | | |
|--------------------------|-----------|-----------------|
| For KB9022 sense 20mΩ | Active | Recovery |
| 45W PR206 2.32K ohm | 58.5W, 1V | Active=recovery |
| 65W PR206 7.87K ohm | 84.5W, 1V | Active=recovery |
| 90W PR20K ohm | __W, __V | Active=recovery |
| PH1 | 2V | 1V |

PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C









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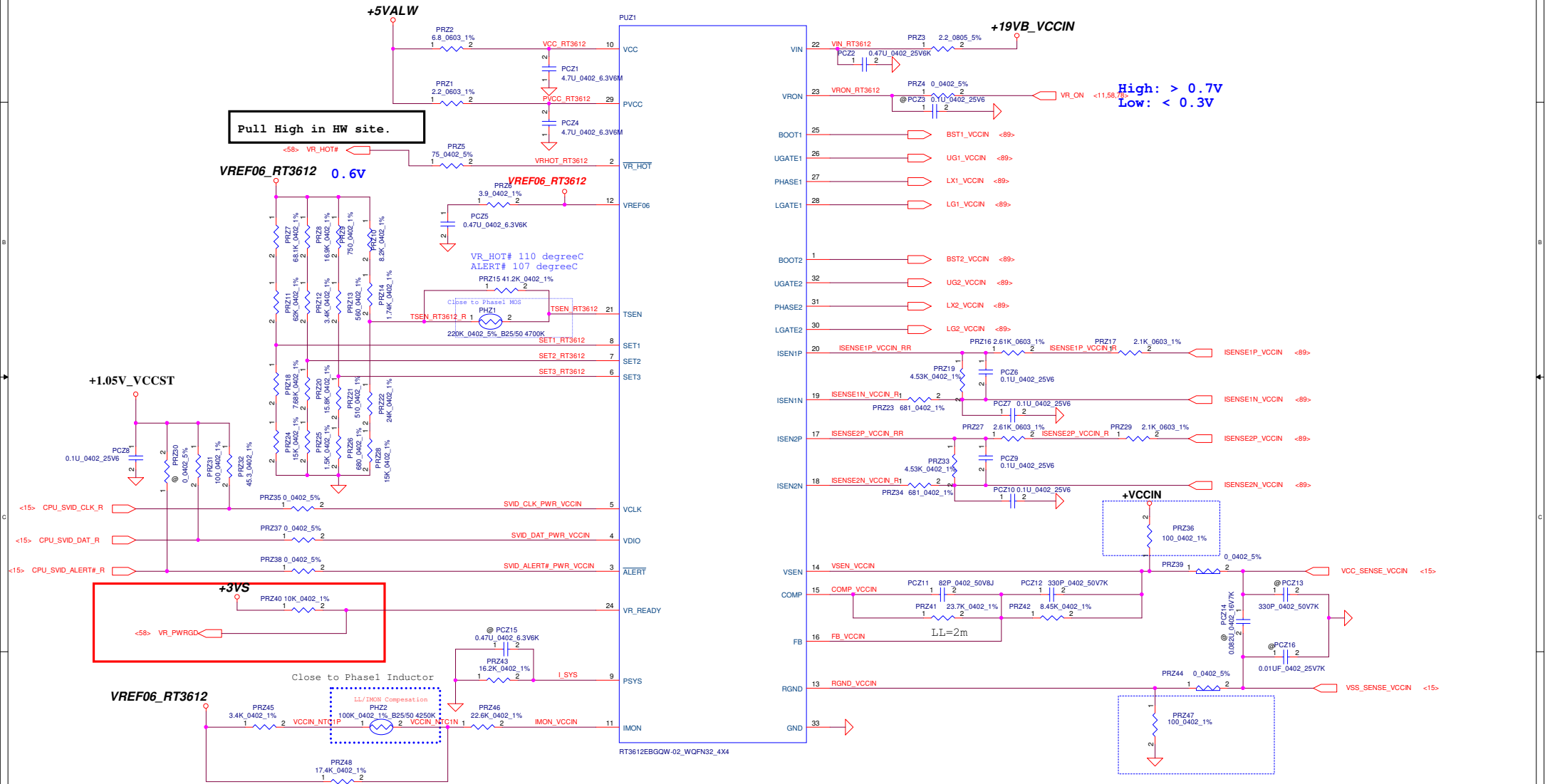
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
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| Issued Date | 2018/12/27 | Deciphered Date | 2019/12/27 | Title | RT8207P |
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Module model information

RT3612EB_2Phase_V1A.mdd for IC portion

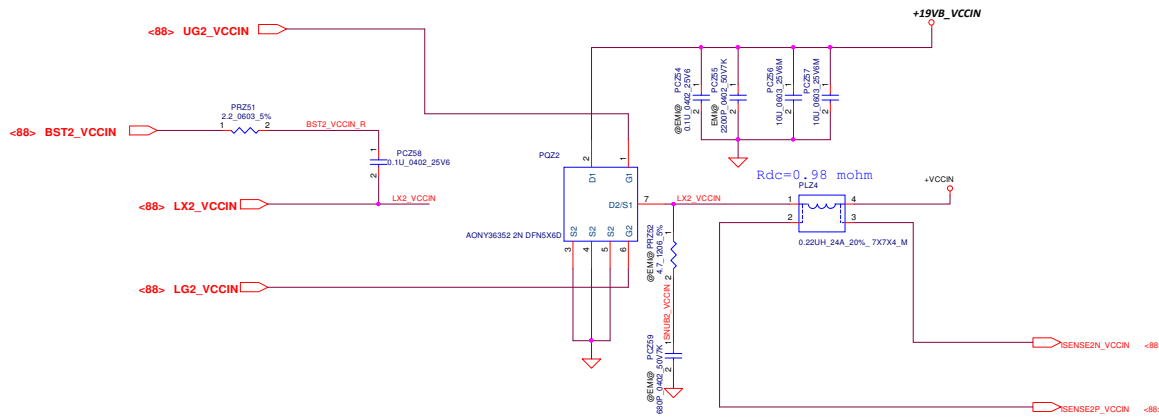
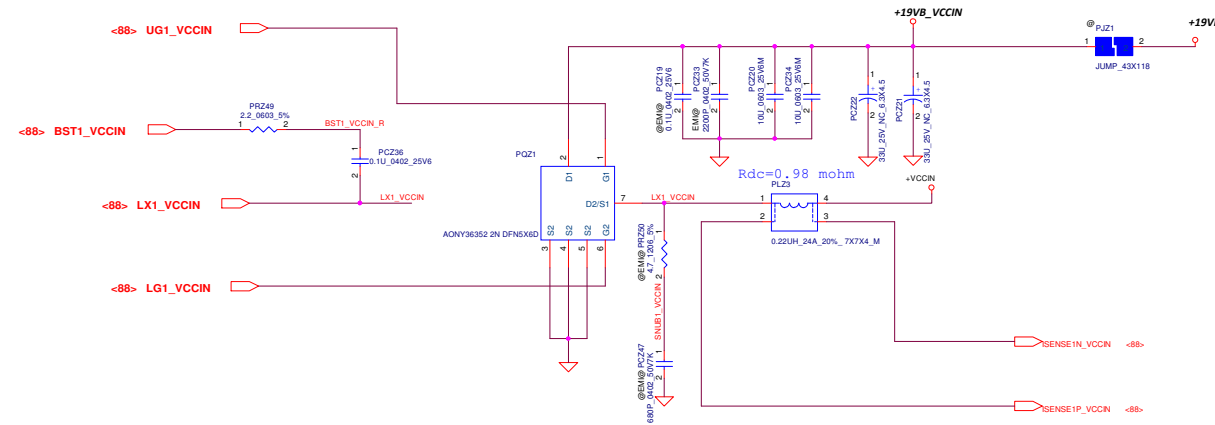
RT3612EB_2Phase_V1B.mdd for SW portion

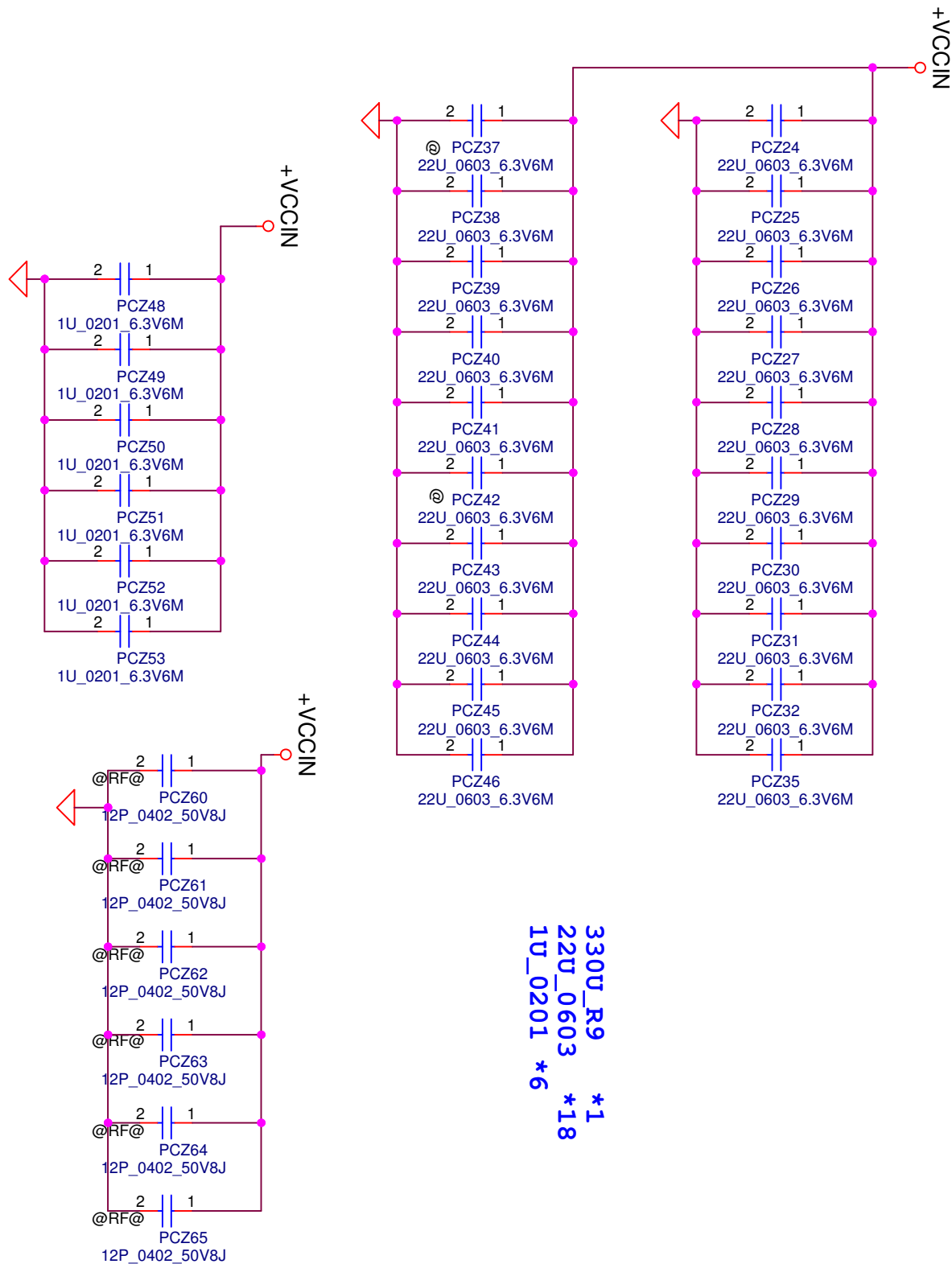
RT3612EBGQW-02 is not MP part



ICCMAX=54A
TDC=25A
OCP=160% of Iccmax=86.4A
OVP=VID+0.35V=2.24V

Frequency 600KHz





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Module model information
RT6543A_V1A.mdd for IC portion
RT6543A_V1B.mdd for SW portion

OCp is Lowside MOSFET Rdson sense

226K x1.2
255K x1.4

+5VALW

High > 1V
Low < 0.4V

+3VALW

+5VALW

5V: 800KHz
Float: 600KHz
GND: 400KHz

VCCIN_AUX VID Follow Intel PDG Rev0.71

| VID1 | VID0 | +VCCIN_AUX Voltage |
|------|------|--------------------|
| 0 | 0 | 0 |
| 0 | 1 | 1.1 |
| 1 | 0 | 1.65 |
| 1 | 1 | 1.8 |

+19VB

AUX input cap need place 5pcs

+19VB_AUX

+19VB

ICCMAX=31A
TDC=14A
DC LL=TBD
AC LL=4.5

Rdc=0.98 mohm

+VCCIN_AUX

+VCCIN_AUX

330U_R9 *1
22U_0603 *13

+VCCIN_AUX

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| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | Date | Phase |
|------|---|--|------|------------|--|----------|-------|
| 01 | Change PCZ21,PCZ22 PN | Avoid material shortage | | P.89 | Change PCZ21,PCZ22 to SF000007700 | 19/09/16 | EVT |
| 02 | Add PRZ36,PRZ47 for CPU transient test | Add PRZ36,PRZ47 for CPU transient test | | P.88 | Add PRZ36,PRZ47 (SD034100080) | 19/09/16 | EVT |
| 03 | CPU transient test | optmization cpu transient test | | P.88 | change PRZ16,PRZ27 to 2.61K(SD014261180) change PRZ19,PRZ33 to 4.53K(SD034453180) | 19/10/09 | EVT |
| 04 | Reduce part count | Reduce part count | | P.84,88,91 | PRB18,PRG2,PRG5,PRG10,PRG11,PRG12,PRG16,PRG25,PRG28,PRZ39,PRZ44 change to R-short | 19/10/14 | EVT |
| 05 | | | | | | | |
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